ESD

APPLICATION HANDBOOK

PROTECTION CONCEPTS, TESTING AND SIMULATION FOR MODERN INTERFACES

Design Engineer's Guide

nexperia

ESD Application Handbook
Protection concepts, testing and simulation for modern interfaces

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Preface

Nexperia is a dedicated global leader in Discretes, Logic, and MOSFET devices. We became independent at the beginning of 2017. Focusing on efficiency, Nexperia produces semiconductor components at high volume, around 100 billion annually. Our extensive portfolio of standard functions meets both the demands of today's state-of-the art applications and the stringent standards set by the automotive industry.

Through our continued efforts in innovation, reliability and support, we maintain the leading position in all our key product segments: diodes and transistors, ESD protection, MOSFETs, and logic devices. We develop and deliver benchmark solutions for today's and tomorrow's market requirements, drawing on a heritage of over 60 years' expertise in semiconductors as the former Standard Products divisions of NXP and Philips.

Our successful record in innovation is the result of varied yet streamlined R&D. We combine the latest technologies with efficient processes, helping us to serve the world's most demanding industries with world-class products.

Nexperia Design Engineers Guides
Our program of Design Engineers Guides allows us to share more technical insights with the engineering community. The first Nexperia Design Engineers Guide, released in 2017, is our MOSFET Application Handbook [1]. In the handbook, our engineers focus on how to use MOSFETs in specific applications and what the key and critical MOSFET parameters are, considering aspects like thermal conditions etc.

The program continues with this Handbook exploring ESD (Electro Static Discharge) and how to minimize the risk of damage it can cause to your circuits.
Why did Nexperia engineers decide to make a guide related to ESD?

We see that ever-increasing data rates, greater calculation power of System-on-Chips, IC miniaturization, and multiple power requirements in confined spaces, are making components and systems ever more sensitive to ESD. Another factor increasing the risk of ESD is the trend to smaller structures of semiconductor processes, because smaller voltages can damage the thinner gate oxide.

Despite all these challenges, the good news is that damages caused by ESD, or EOS (Electrical Over Stress), can be avoided or at least massively reduced with an optimized ESD protection concept. To this end, Nexperia's ESD competence can help minimize the risk of ESD damage — supporting the design community in protecting applications and products against ESD issues.

This "ESD Application Handbook" is a prime example of Nexperia's commitment to Standard Products, and of our endeavor to share technical insights and guidance to support our customers' needs. Inside you will find invaluable information about ESD testing and the principles of ESD protection and EMI filtering, together with application examples with an emphasis on communication bus interfaces. Due to their susceptibility to ESD damage and EMI interference, interfaces are the natural focus of this guide and it covers many popular types found in all products from mobile to automotive.

Olaf Vogt

Director Application Marketing
Nexperia

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Chapter 1
Introduction

Shrinking silicon geometries allow more complex electronic content to be squeezed into small spaces. With these new silicon processes oxide layers have become thinner and the gates of embedded FETs are therefore more vulnerable to surge events. High voltage events of up to 30 kV peak voltage with about 100 ns overall pulse width resulting from electrostatic discharges (ESD) must be considered as well as surge events with a longer pulse width of about 60 µs and less extreme voltage levels.

Often, designers can no longer rely on the internal ESD protection structures of the system chips. Internal ESD protection is good enough to protect the components during the assembly process in a mostly ESD safe environment. It does not protect against ESD events seen in the field. External protection cannot be seen as a luxury or left out.

In computing, consumer, and mobile products, super-speed interfaces conquer the market where huge quantities of data are transferred or copied in a short time. The automotive industry introduced many Electronic Control Units (ECUs) that are connected via networks exposed to ESD strikes and surge events potentially induced from high-current switching over long cables, load dump conditions, or voltage changes from cold car cranking.

All modern high-speed and super-speed interfaces use differential data signals and operate with reduced signal levels. High data speed, up to 20 Gbit/s, requires a carefully designed PCB layout to maintain signal integrity. This can be achieved by proper impedance matching, avoiding unacceptable losses and reflections. Various electromagnetic interference (EMI) aspects also need to be considered when sensitive GSM, WiFi, or GPS receivers are located close to potentially radiating high-speed interfaces.

This handbook provides information about the physical layers for selected data interfaces used in mobile, computing, and consumer applications as well as for interfaces that can be found in automotive applications. These layer specifications are relevant for the selection of adequate ESD protection, to maintain signal integrity, and to choose the most suitable ESD diode topology respecting signal levels and the structure of drivers and receivers.

Findings for latest generation super-speed interfaces and practical knowledge how to get these extremely sensitive interfaces properly protected with high system level robustness are presented. Furthermore, different ESD and surge protection topologies and their major application areas are discussed.

The key parameters found in datasheets are explained in detail and how to choose a suitable component for a design based on this information. Various testing standards have been established to allow reproducible testing and qualification of electronic components and products. The most important testing methods are discussed in this handbook and how to use the 'new' Transmission-line pulse (TLP) testing method. It introduces a scientific selection process for ESD protection devices, overcoming the time-consuming trial and error testing that does not necessarily find the best solution.

In addition, the handbook introduces the so-called System efficient ESD design (SEED) methodology to simulate ESD behavior of ESD protection devices and system chip interfaces as individual blocks as well as in combination to judge if the two components will fit together and are safe against ESD and surge events.

1.1 Overview of most important interfaces

Interfaces with external connectors accessible to users require the highest attention to be safe against electrostatic discharge and surge events. The most important wired high-speed multimedia interfaces in the market are shown in Figure 1. An ongoing increase in the maximum supported data rate can clearly be seen. This is not achieved with more parallel data connections but with a higher bit rate on the data lines, which has a significant impact on the requirements for ESD protection as discussed in depth in Chapter 8.

Interface	Data rate	Application area
THUNDERBOLT	20 Gbit/s	All applications areas
SUPERSPEED USB	10 Gbit/s	All applications areas
DP	8.64 Gbit/s	HD audio/video data, Consumer/computing
mipi alliance	6.9 Gbit/s	Mobile data interfaces, All applications areas
HDMI	6 Gbit/s	HD audio/video data, All applications areas
APIX	0.5–3 Gbit/s	e.g. for flatscreens, camera data, In automotive applications
HI-SPEED USB	480 Mbit/s	USB 2.0, legacy mode, All applications areas

**Figure 1** | Multimedia Interfaces

- Universal Serial Bus (USB) specifications USB 2.0 and its successor USB 3 generation 1 and 2, have dominated all application areas like mobile communication, computing, consumer, and automotive infotainment. USB interfaces certainly require ESD protection because of the regularity of connecting and disconnecting devices by end-customers. More details can be found in Section 8.1.

- APIX is found in automotive application as flat-screen or camera data interface.

- High Definition Multimedia Interface (HDMI) is one of the major video/audio interfaces in consumer applications. It has achieved a high relevance for computing applications for monitor connection, supporting video and audio data transfer in parallel. Resolution in terms of pixels per frame and quantization of video data has increased over time. HDMI data lines are DC-coupled which makes this interface somewhat special for ESD protection as discussed later in this handbook. For more details see Section 8.2.

- Display Port (DP) is an alternative connection for HDMI and important for the computing market, it also supports high display resolutions.

- MHL (Mobile High definition Link), with similarities to HDMI, is used in some mobile devices and TV sets but as yet has not gained significant market share.

- Mobile Industry Processor Interface (MIPI) is mainly an internal interface for mobile processors to cameras, memories, displays and sensors. It has a high relevance in smartphones and although an internal interface, ESD protection can be found in many designs. More details can be found in Section 8.3.

- Thunderbolt interfaces are gaining importance with the introduction of Type-C connectors. Type-C connection can support different data interface standards as a new hardware platform of a miniaturized connection. Following the fully established USB interface Thunderbolt can gain market share in the computing market. It has the very high physical data speed of 20 Gbit/s. Usually, ESD protection suitable for USB super speed lines can be applied for Thunderbolt as well.
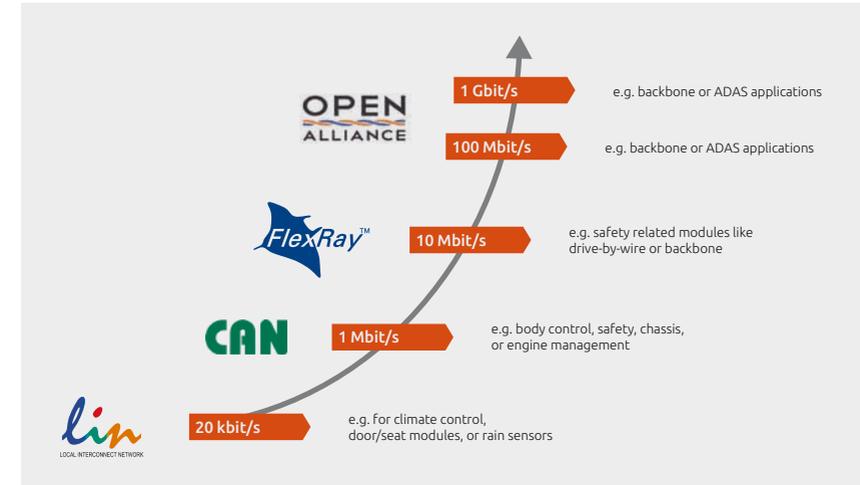
Figure 2 | Automotive Interfaces

Figure 2 shows dedicated data interfaces for automotive applications including LIN, CAN and FlexRay. Like the multimedia interfaces data speed constantly increase to support the growing electronic content in modern cars. A more detailed overview is provided in Section 8.4.

In addition to the digital interfaces mentioned above, ESD protection of antenna inputs is a special application area discussed in Section 8.5 of this handbook, along with surge protection of DC supplies in Section 8.6.

1.2 Three key parameters for a suitable ESD and surge protection

Regardless of the application or interface, when choosing an ESD protection strategy, there are three essential parameters. The first is a high robustness of the protection device itself against ESD and surge events. Another requirement is a low clamping voltage with a low dynamic resistance. A low dynamic resistance stands for a steep I-V-curve of the protection, so that clamping voltage does not increase much if surge current is increased. These requirements are extremely important to achieve a high system level robustness - the primary goal of why ESD and surge protection is applied.

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As a third key parameter, a low capacitance of the ESD protection device is required if high data rates need to be handled. Low capacitance is key to maintain excellent signal integrity. From a design perspective, trying to maximize one parameter can result in a deterioration of another. Figure 3 shows the three discussed key parameters and their relevance for different application areas.
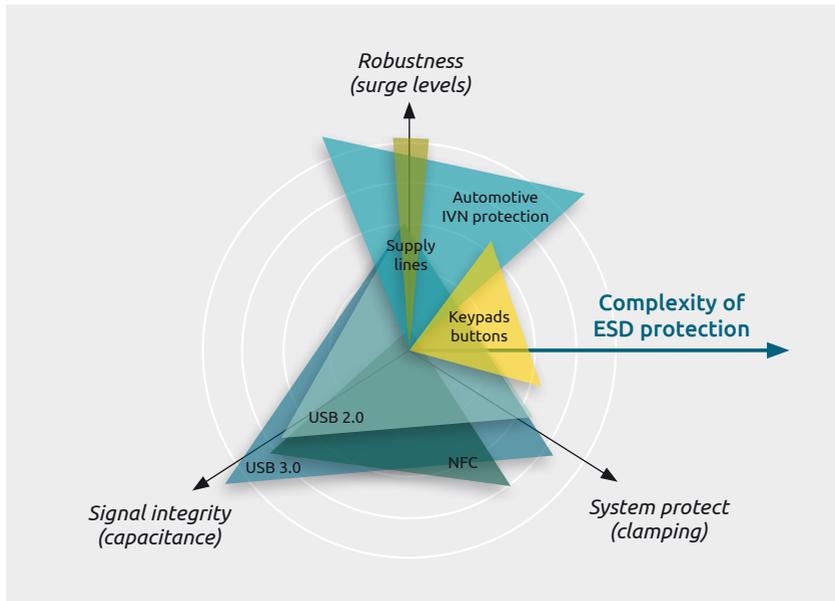
Figure 3 | Challenges in protecting interfaces

Under the name TrEOS Protection Nexperia is offering an ESD protection technology that combines benchmark values for all three key parameters – deep snap-back, low dynamic resistance and high ESD robustness with very low capacitance. This technology is ideally suited for super-speed data lines such as RX/TX lines of USB 3.2 or Thunderbolt interfaces and to protect very sensitive SoCs.

Chapter 2

Datasheet parameters of ESD protection devices

2.1 Introduction to datasheet parameters

To select suitable ESD protection devices, development engineers have to compare key parameters that can be found in vendor datasheets. In this chapter the most important key parameters and their relevance for a well operating interface are described. Furthermore, the signal integrity has to be maintained to ensure that receiver circuits in digital interfaces can sample the incoming data without errors. The following chapters are clustered like the information in most datasheets for ESD protection devices by Nexperia.

2.2 Limiting Values

V_{RWM} is the standoff voltage of a protection device. It indicates the maximum operating voltage range for which leakage current is below a specified value I_{RM}. V_{RWM} has to be equal to or higher than the maximum voltage expected on a signal line.

I_{PPM} is the maximum surge current that a device can withstand if an IEC 61000-4-5 [2] pulse with an 8/20 µs timing is applied. This value gives an indication of the robustness of ESD devices if they are exposed to higher pulse energy, see Chapter 3.3.

For the junction temperature T_j, a maximum value is given which usually is 150°C. Beside this information, an ambient temperature range T_{amb} and storage temperature T_{stg} can be found with minimum and maximum limits.

2.3 ESD maximum ratings

V_{ESD} gives the maximum voltages that an ESD protection device can withstand, in compliance with IEC 61000-4-2 [3], see Chapter 3.2. The limits in kV are given for positive and negative ESD test pulses. The datasheets give limits for contact discharge testing as well as for air discharge testing. For low capacitance protection devices, the air discharge rating is not significantly higher than the contact discharge rating. Designers should rely on the contact discharge rating because this is much better in reproducibility. The ESD rating does not indicate if a protection device will provide good protection for an interface. It has no correlation to the ESD system robustness that can be achieved. In the best case, the overall system robustness is limited by the ESD robustness of the ESD protection device.

However, this is not the case in most applications if sensitive interface pins have to be protected. If the system chip is damaged with an 8 kV ESD pulse in a system test, it does not help that an ESD diode with a +/− 30 kV rating was applied. A low clamping protection diode rated for e.g. 15 kV can be the far better choice.

2.4 Characteristics

The diode capacitance C_d is an important parameter related to the maximum frequency of a signal line. The value is given for a test frequency of usually 1 MHz and no bias; sometimes, additional values with bias voltage are provided. A bias voltage leads to lower C_d values because the capacitance of internal pn-junction, decrease with reverse voltage.

f_{-3dB} is the −3 dB frequency of the insertion loss tested at a sine-wave generator with 50 Ω output resistance. Figure 4 shows an example for an insertion loss curve with a −3 dB cut-off frequency of about 17 GHz. For data interfaces, at least the fundamental wave should pass without big losses. To achieve steeper transitions, it is essential to have a significant spectral component for the 3rd harmonic as well.


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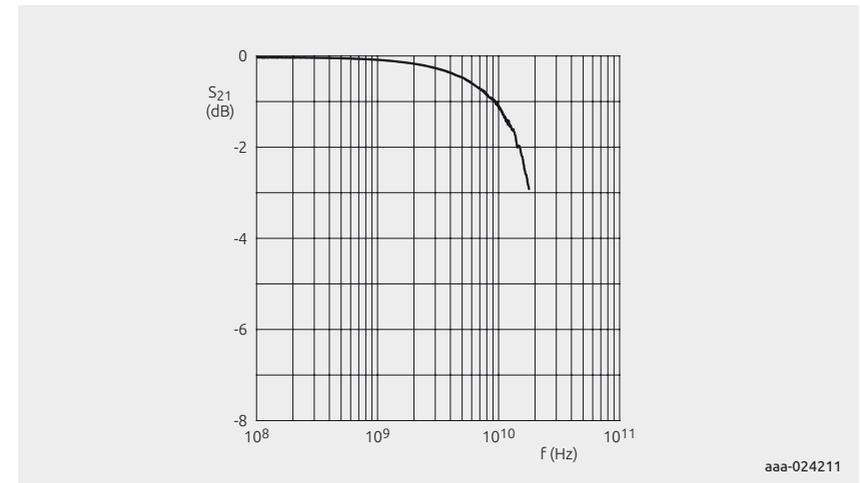
Figure 4 | S_{21} insertion loss curve of PESD3V3Z1BSF

V_{BR} is the breakdown voltage of a protection device. It is tested with a current-driven set-up in which 1 mA test current is driven through the DUT. The voltage across the DUT is V_{BR}.

For a topology similar to an ordinary Zener diode, this parameter is of practical interest as it indicates the voltage at which leakage current will reach 1 mA. However, for ESD protection that has a snap-back topology but not static behavior, V_{BR} can be misleading. ESD protection devices with an open-base topology have very low leakage currents below 1 mA before the trigger voltage is reached. The current-driven test approach for V_{BR} forces such devices into snap-back. In this case V_{BR} is lower than the trigger voltage and V_{RWM} can be higher than V_{BR} in principle.

I_{RM} is the leakage current at V_{RWM}. It is typically extremely low, at 1 nA and a maximum rating of 50 nA.

V_{CL} are clamping voltages for IEC 61000-4-5 pulses for different peak currents I_{pp}. Usually V_{CL} is given for the limiting I_{pp} value and additional lower values.

R_{dyn} is the so called dynamic resistance. For modern devices this parameter is defined by the steepness of the TLP curve for TLP pulses with 100 ns pulse width at $I_{PP} \sim 16$ A. The lower the dynamic resistance of a protection device, the better is the clamping performance. This is because the clamping voltage increases less for rising surge currents. In many datasheets, dynamic resistances are given based on IEC 61000-4-5 (8/30 µs pulses) test results. The value is derived from an I_{PP} (peak current) versus clamping voltage curve for such a test. When comparing dynamic resistances, attention has to be paid to the test method, because the values are not identical for the two approaches due to the significantly higher energy of IEC 61000-4-5 pulses towards TLP testing.

S-parameters

A scattering, or S-parameter, matrix is a mathematical approach that quantifies how RF energy propagates through a multi-port network [16]. The S-parameter matrix allows the properties of a complicated network to be described as a simple black box with n ports. The matrix for a network with n ports contains n² coefficients, each of them representing a possible path.

S-parameters are complex numbers containing real and imaginary parts, or a magnitude and phase part. The network changes both the magnitude and phase of the incident signal. S-parameters are defined for a given frequency and a defined system impedance Z_0, which is 50 Ω for datasheets and Nexperia laboratory testing. S-parameters are measured over a chosen frequency range and vary over frequency, as Figure 4 shows with the example of an S_{21} parameter curve.

S-parameters are usually depicted in a matrix format. The number of rows and columns is equal to the number of ports. For the S-parameter S_{mn} the n subscript stands for the port that is excited, as input port. The m subscript stands for the output port. This means S_{11} describes the reflection on port one: It is the relativ signal amplitude that is reflected. Parameters in the S-matrix diagonal are the reflection coefficients, while those located off the diagonal are called transmission coefficients. They describe how the network reacts at a port if it is excited with an incident sinewave from another port. The parameter S_{21} is often referred to as insertion loss.

S-parameters describe the response of an n-port network to a signal incident to any or all of the ports.
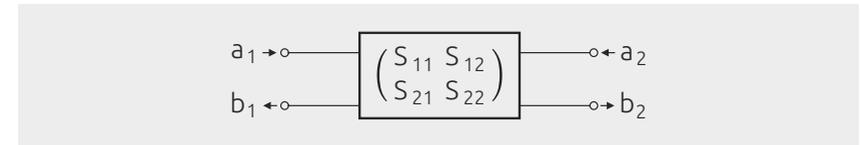
Figure 5 | 2-port network with 4 nodes and direction indication arrows

Figure 5 shows a 2-port network. The signal at a port, for example port 1, can be thought of as the superposition of two waves running in opposite directions. By convention, each port is shown as two nodes so as to give a name and value to these opposite direction waves. The variable a_m represents a wave incident to port m and the variable b_n represents a wave reflected from port n. From the matrix formula below the following equations are valid for the four S-parameters of the 2-port network:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \cdot \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}$$

$$S_{11} = \frac{b_1}{a_1}, \ S_{12} = \frac{b_1}{a_2}, \ S_{21} = \frac{b_2}{a_1}, \ S_{22} = \frac{b_2}{a_2}$$

Datasheet parameters of ESD protection devices

Chapter 3

ESD testing standards and TLP testing

3.1 ESD testing standard IEC 61000-4-2

IEC 61000-4-2 defines test methods and configuration environment for ESD robustness testing [3]. It is commonly used to certify electronic equipment. Devices must be protected against ESD using components that can clamp and resist the high voltages, as defined by the respective IEC standards. The robustness of these devices has to be checked and guaranteed.

Most electrostatic discharges occur unnoticed by users but can seriously damage gate oxides of MOSFETs used in the data path of most interfaces. In some cases, a small flash indicates that a sudden electrical discharge has occurred. The after-effects are high leakage currents and malfunction of input and output circuits.

Contact and rubbing of different materials causes seperations of charger by means of the socalled triboelectric effect. Furthermore, electrostatic induction leads to a redistribution of electrical charge in an object caused by the influence of nearby charges.

Please note that when ESD protection components are mounted in a product to protect some of its sensitive parts, the behavior of these components must be tested in their final application environment. ESD pulses are generated with an ESD gun that consists of an adjustable high voltage source with maximum of 30 kV. A 150 pF capacitor is charged through a resistor with 50 to 100 MΩ, using a charging switch. The capacitor is discharged through a 330 Ω resistor when the discharge switch is closed. Figure 6 shows a basic ESD pulse generator schematic.
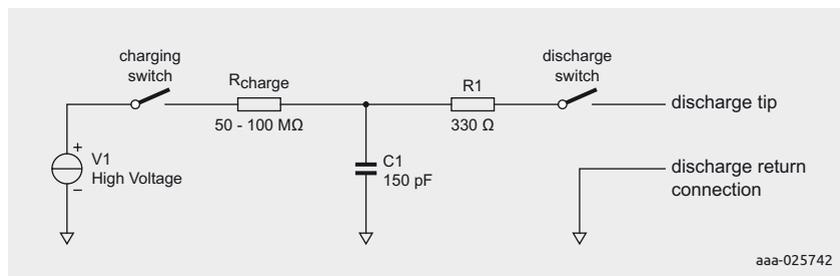
Figure 6 | ESD pulse generator according to IEC 61000-4-2

Figure 7 shows the shape of the IEC 61000-4-2 discharge current waveform of the described generator. The curve behaves in the following way:

1. The pulse rises within 0.7 to 1 ns.
2. The first spike reaches its peak current with the peak value I_{PP}.
3. The pulse then declines within about 80 ns including a shoulder-shape curve.

Most of the surge pulse energy is carried by the shoulder. The first spike stresses the target with high voltage and high current, but with less energy because duration is short. Two methods are used for ESD testing: The contact measurement method and the air discharge measurement method.

The contact measurement method is the recommended IEC 61000-4-2 method for ESD protection components and is set-up as described below:
- The ground pin of the component is connected. The ESD gun is connected to ground via the discharge return connection as well.
- The tip of the ESD gun is connected to the contact of the device under test (DUT).

In contrast to the system level testing described in IEC 61000-4-2, the test procedure of ESD protection devices does not employ resistors (2 × 470 kΩ) in the return path. The contact discharge connection allows good reproducibility of test results. Further details on the test procedure can be found in [5].

Table 1 lists current values for predefined IEC 61000-4-2 levels, i.e. ESD levels 1 to 4, for respective peak currents, 30 ns and 60 ns.
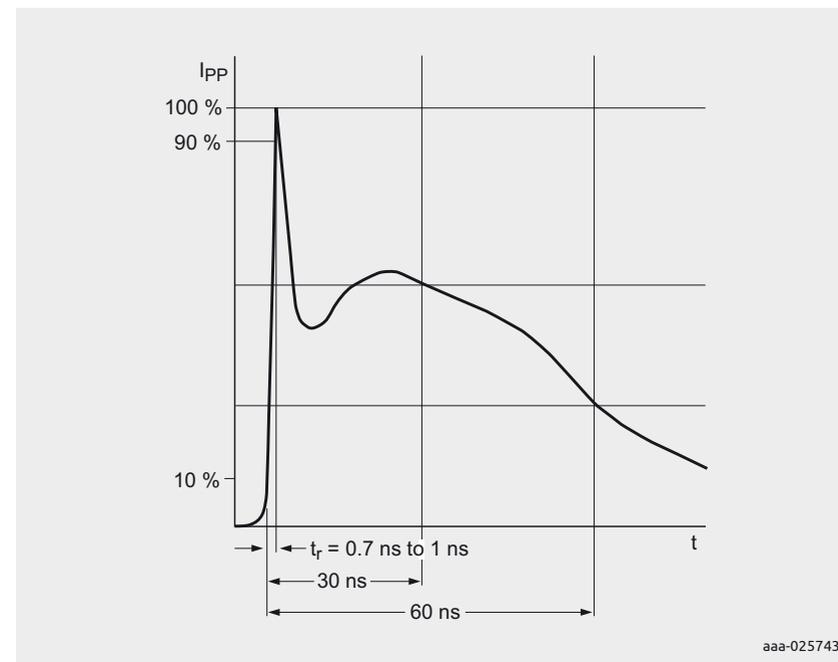
Figure 7 | IEC 61000-4-2 waveform

Table 1: ESD test waveform parameters

ESD level	voltage	first peak current, +/− 10%	Current (+/− 30%) at 30ns	Current (+/− 30%) at 60ns
1	2 kV	7.5	4	2
2	4 kV	15	8	4
3	6 kV	22.5	12	6
4	8 kV	30	16	8

Table 2 shows the definition of IEC 61000-4-2 ESD levels with the related minimum discharge voltages for contact discharge testing.

Table 2: ESD levels as defined in IEC 61000-4-2

| ESD level	contact discharge	air discharge
1	2 kV	2 kV
2	4 kV	4 kV
3	6 kV	8 kV
4	8 kV	15 kV

For air discharge the tip of the ESD gun is narrowed slowly towards the target until a flash strikes over. The results depend very much on air humidity, speed of decreasing distance between target and gun, and shape of electrodes. Generally this test shows low reproducibility. Often, corona discharge can be noticed without a flash if one of the two electrodes has a sharp end. In such a case, the stress on the ESD device is very low and does not lead to usable results. For the gun side a tip with a round end is defined for air discharge, whereas the tip for contact discharge has a sharp end. The air discharge waveform has a less steep rising edge and the surge pulse peak values are lower. Therefore, **air discharge robustness is higher than, or equal to, contact discharge**.

Please note that technical documents must be regarded with skepticism if air discharge ratings are presented with much higher values than for contact discharge. Often, a factor of roughly 2 like the ESD level 4 definition in Table 2 is presented. Please note that the voltage levels do not imply each other, but are just categorizations for practical usage. Moreover, the levels defined in [3] refer to system level testing rather than device level. It is a proven fact that for low capacity ESD protection devices the air discharge robustness is a few kV higher or the same compared to contact discharge robustness. For this reason air discharge testing is discouraged not recommended, because it is much more difficult to do it correctly and, if done correctly, it provides exactly the same results as contact testing [32].

Human Metal Model (HMM) test uses the same waveform as defined for ESD guns in standard and supports 50 Ω terminated testing of ESD protection products and interfaces. The defined termination guaranties good reproducibility of test results as known from TLP tests.

3.2 Reproducibility aspects for IEC 61000-4-2 testing

Figure 8 shows that the ESD gun waveform is not fully reproducible: Here, a NoiseKen gun[1] is shooting in repeat mode at a target while a high frequency current probe[2] is measuring the current waveform. The second peak, which is located on the shoulder behind the first peak, is stable and is well within the IEC 61000-4-2 specification. However, the voltage of the first peak shows a big variation from +25% to −35%. If target systems are sensitive to the first peak of an ESD event, test results can show a big spread which can lead to wrong decisions being taken in the selection process of protection devices. Guns of other manufacturers show simular behaviour.

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1 ESS2000AX
2 F-65 current probe 1 MHz–1 GHz from Fischer Custom Communications
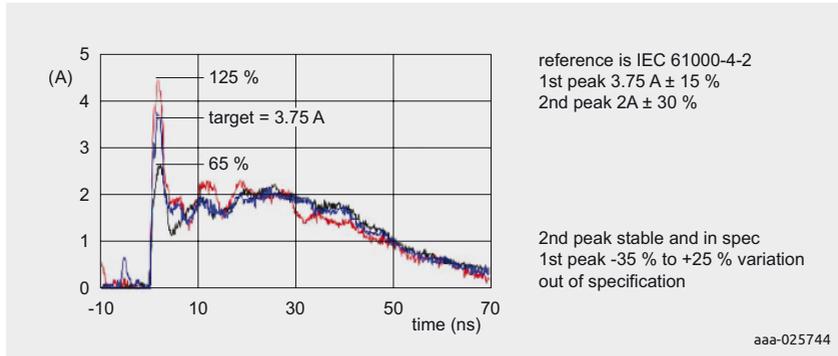
Figure 8 | IEC 61000-4-2 waveforms with NoiseKen ESS2000AX gun

Please note that the grounding condition has a big impact on the voltage level of the first peak as well. If there is no proper ground close to the DUT, a small residual capacitance to ground occurs. If this is the case, the first peak loses its height and can mostly disappear. Figure 9 shows the current waveforms of two ESD gun[3] types with and without proper grounding. In set ups without proper grounding test results are unreliable.
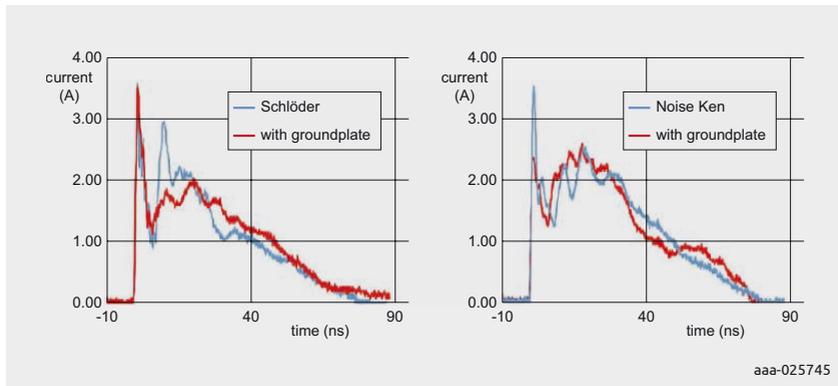

Figure 9 | Waveform comparison for ESD gun with and without proper grounding

Another risk in ESD gun testing arises when the gun is not safely connected to the DUT for contact discharge. Figure 10 shows the circuit of an ESD gun with a parasitic tip capacitance C_t of roughly 40 pF, which is significant compared to the nominal 150 pF of the ESD gun.

3 A SESD 30.000 from Schlöder and a ESS2000AX from NoiseKen

When a triggered gun misses the target or when the charge moves across the switch S2, the C_t charge can discharge into the DUT with almost no series impedance. This is why the first peak of this socalled stray pulse can exceed the regular pulse by a factor of 2, as illustrated by the red curve in the diagram.

In conclusion, if a system is tested that shows an ESD sensitivity on the first peak, unsafe ESD gun connection can lead to damage at a comparatively low testing voltage, wrong test results, and ESD device selection. A propper test setup is essential to ensure reproducibility of ESD testing. More details about system level ESD testing of high-speed interface boards can be found in [16] and [33].
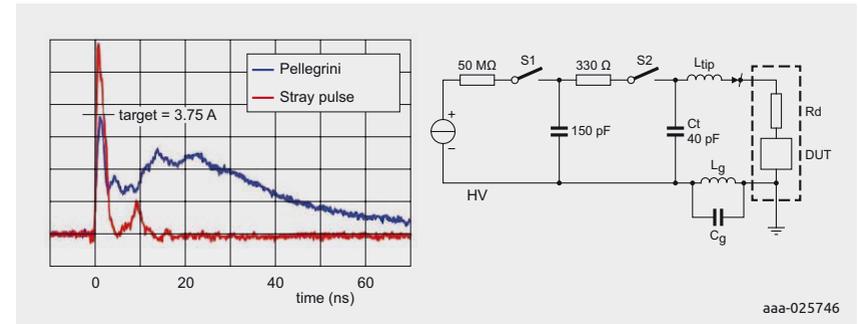
Figure 10 | Stray pulses after the target was missed

3.3 Surge testing standard IEC 61000-4-5

Testing according to IEC 61000-4-5 [2] uses much wider test pulses than in the ESD testing according to IEC 61000-4-2 [3] discussed in the previous chapter. The energy of surge pulses, as defined in [2], is much higher. Consequently, an ESD protection part has to dissipate more heat. The IEC 61000-4-5 standard approach simulates surge events, for instance in scenarios like power supply voltage overshoots created by load changes or overshoots caused by the plug-in procedure of chargers.

Table 3 lists key waveform data of IEC 61000-4-5 surge pulses. For the short-circuit condition of the surge generator, see Figure 12, 8 μs rise time and 20 μs fall time to 50% voltage level are defined and is well known as the 8/20 μs surge test.

Table 4 lists the relation between selected values of the peak voltage for the open circuit condition, see Figure 11, and the peak current for the short circuit case. Output impedance of a surge generator is considered to be 2 Ω.

Table 3: Surge pulse waveform parameters

operating mode	Front time in µs	time down to 50% value in µs
open-circuit voltage	1.2 +/− 30%	50 +/− 20%
short-circuit current	8 +/− 20%	20 +/− 20%

Table 4: Open-circuit peak voltage and related peak current for the short-circuit

open circuit peak voltage +/− 10%	short-circuit peak current +/− 10%
0.5 kV	0.25 kA
1.0 kV	0.50 kA
2.0 kV	1.00 kA
4.0 kV	2.00 kA

Figure 11 shows the waveform for the open circuit condition, whereas Figure 12 depicts the surge pulse waveform for the short circuit scenario.

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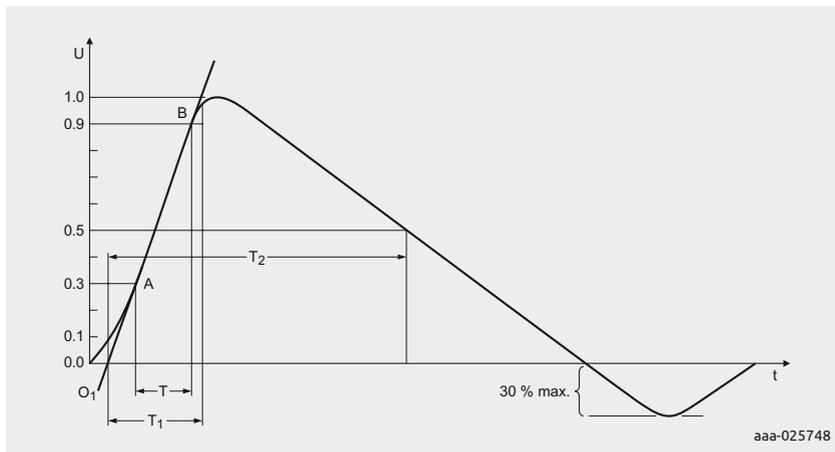
Figure 11 | IEC 61000-4-5 waveform for open circuit condition

Front time: $T_1 = 1.25 \times T = 8$ µs ± 20 %
Time to half-value: $T_2 = 20$ µs ± 20 %

aaa-025749
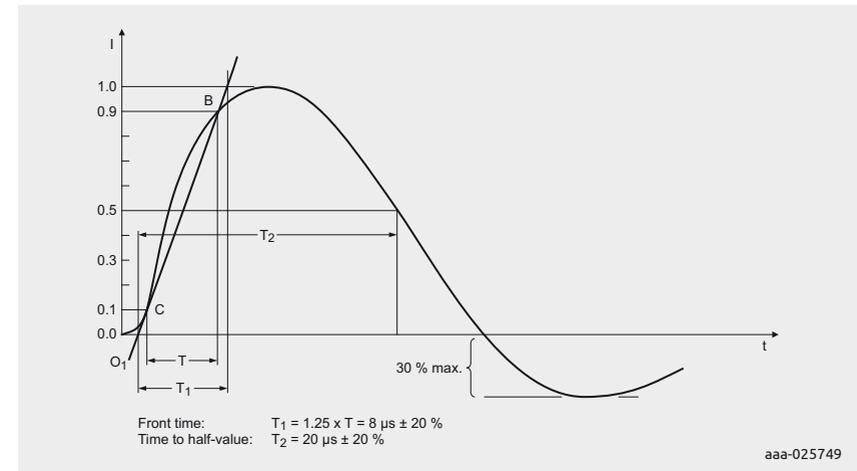
Figure 12 | IEC 61000-4-5 waveform for short circuit condition

IEC 61000-4-5 test results deliver important data sheet parameters for ESD and surge protection devices:

- Maximum surge current — I_{PP}
- Peak power — P_{PP}
- Clamping voltage — V_{CL}
- Dynamic resistance — R_{dyn} — derived from the steepness of V_{CL} versus I_{PP} curves

3.4 Transmission-Line Pulse (TLP) testing

TLP is a comparatively new measurement technique used to characterize complete interfaces or ESD protection components [4,5].

TLP is a short-duration rectangular pulse in a controlled impedance environment of 50 Ω, which improves test accuracy and measurement reproducibility. TLP characterizes performance attributes of devices under stresses that have a short pulse width and fast rise time. Low duty cycles prevent heating.

The TLP test environment shown in Figure 13 can be described as follows: a generator charges a 50 Ω transmission line with a pre-adjusted voltage. The switch is closed and the energy is applied to the DUT. The current into the DUT measured by a current probe, while the voltage at the DUT is monitored using a high-speed oscilloscope. The pulse length, rise, and fall times can be changed at the generator. Typically, the standard pulse applied has a 100 ns duration and rise and fall times of 10 ns each. The minimum programmable transition times are 300 ps.

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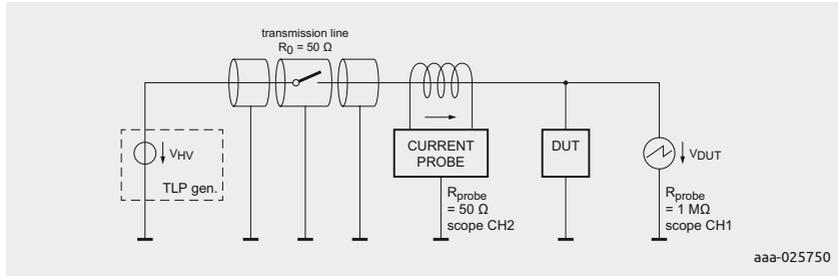
Figure 13 | TLP test set-up

The TLP test is performed starting gradually from low pulse voltages to higher voltages, with a pre-defined step width. As shown in the TLP measurement voltage and current traces depicted in Figure 14, the voltage and current samples are averaged for a window of 20 ns. Located in a temporal window from 70 ns to 90 ns within the 100 ns test pulse, the window-based method eliminates noise. Also, the window's location ensures that the system is settled so that run-in effects like overshoots are eliminated. Each measurement result becomes a point on the TLP graph that shows a TLP I-V characteristic, i.e. the TLP-curve.

The steepness of the TLP curve ΔV/ΔI is the R_{dyn}, which is an important parameter for selecting ESD and surge protection devices.

TLP testing can be done with ESD protection devices, and with interface pins of complete systems with and without ESD protection. From the derived TLP curves conclusions can be drawn as to which protection device is suitable to protect a product safely and reliably.

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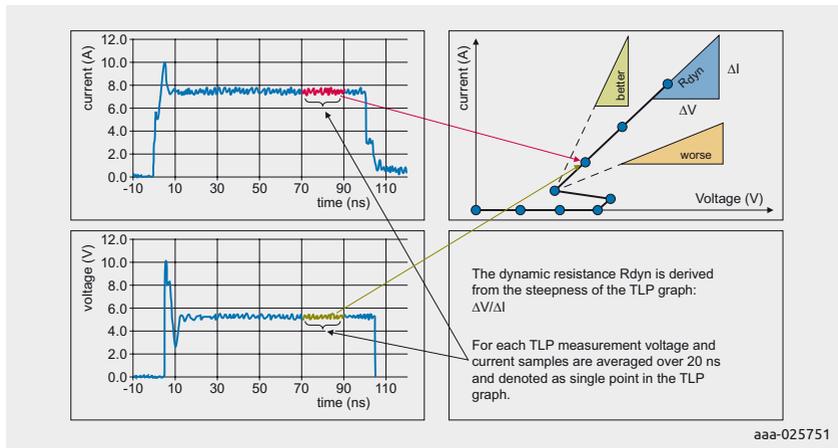
Figure 14 | TLP curve derived from TLP test events

3.5 Very fast TLP (VF-TLP) testing

A very similar testing method to TLP is very-fast TLP (VF-TLP) [6]. The major differences being the 1 to 10 ns duration of the test pulses and the short rise and fall times of 100 to 600 ps.

Figure 15 shows the VF-TLP measurement set-up. Due to short pulses, the current is not measured with a current probe. Instead, it is derived from measuring incident and reflected voltages separately with an oscilloscope. This is done in a similar way to time domain reflection (TDR) measurement. The current in the DUT is calculated using:

$$I_{DUT} = I_{incident} + I_{reflected} = \frac{V_{incident} - V_{reflected}}{50 \ \Omega}$$

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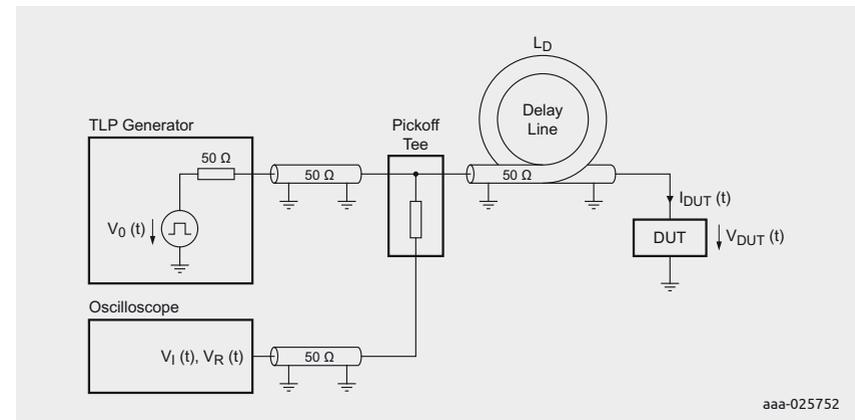
Figure 15 | Test set-up for VF-TLP measurement

In conclusion, VF-TLP tests provide a good indication for determining the switching speed of ESD protection devices. The small pulse length is useful because the impact of the first overshoot of an ESD event on a target system can be investigated.

In contrast to that, the 100 ns standard TLP pulses are roughly equivalent to the energy of a complete ESD pulse, in which the larger proportion of energy is carried in the wider second shoulder of the pulse.

Chapter 4

Principles of ESD protection

4.1 Introduction into ESD protection choices

Several different approaches can be used to protect electronic devices against ESD and surge events.

- **Narrow gap or spark gap approach**
  An easy and inexpensive approach is to add a narrow gap from ground to signal line. Whenever a bigger ESD event occurs, an air discharge limits a high voltage pulse.
  Spark gap components operate on the same physical principal. Thus, adding a spark gap to a signal line is a straightforward approach. The disadvantage of this kind of ESD protection is comparatively poor performance in terms of the achieved clamping voltage that has a slow turn-on time and a very high trigger voltage. The average dielectric air strength is about 3.3 kV/mm. This is why a spark gap is not a good protection device choice for modern high-speed interfaces.

- **Use of varistors**
  Varistors are often used for ESD protection. These parts are made with ceramic ZiO grain material in a mixture with other metal oxides. Varistors have a symmetrical non-linear I-V curve which shows a high resistance for lower voltages. When the varistor reaches breakdown voltage, it starts conducting. Varistors deteriorate after exposure to surge events. Older generation varistors show a very high first spike in IEC 61000-4-2 testing, however newer generation varistors are much improved. Unfortunately, the clamping voltage for the second shoulder remains significantly higher compared to silicon-based solutions. This is why varistors are not the first choice for protecting modern system chip interfaces.

- **Silicon-based ESD protection**
  Silicon-based ESD protection are the preferred choice as they show no degradation after surge events, as long as the specified limits are obeyed. Several topologies are available that provide ESD protection ranging from a simple topology, as presented in Figure 17, to more sophisticated topologies, as presented in several scenarios on the subsequent pages.

Silicon-based ESD protection is recommended with best and lowest clamping voltage performance, as explained on the subsequent pages of this section.

4.2 Unidirectional ESD protection with a Zener diode

A very plain topology is a Zener diode placed between ground and signal line, as depicted in Figure 16. Surge pulses are clamped to a voltage V_{CL} that is based on the following V_{CL} equation:

$$V_{CL} = V_{BR} + I_{PP} \cdot R_{dyn}$$

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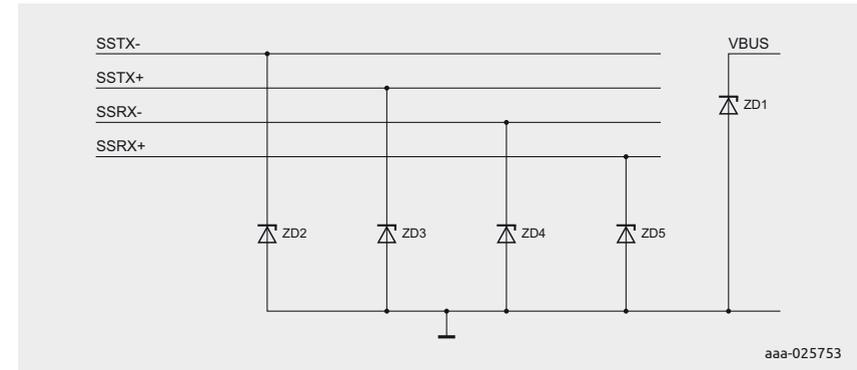
Figure 16 | ESD protection based on Zener diodes

Figure 17 shows a typical Zener diode I-V curve. The left side of the curve shows the Zener diode in the reverse bias region. The current is very small, as long as the test or operating voltage remains below V_{RWM}. V_{RWM} is referred to as stand-off working voltage. Below this voltage, reverse leakage current is smaller than the specified I_{RM}. When the voltage increases, current increases suddenly, at which the avalanche region begins; marked by the breakdown voltage V_{BR}. The breakdown voltage is measured in a current-driven test set-up that pushes 1 mA through the diode.

The right side of the curve shows the Zener diode in the forward bias region. The current is picking up if the voltage exceeds V_F. Negative surge pulses are clamped to relatively low voltages (V_F –0.7 V). The described topology forms a unidirectional protection.

A Zener diode creates a unidirectional protection for an interface, clamping at considerably low voltages for negative surge events above V_F, as well as clamping voltage — according to the V_{CL} equation — for positive surge events.

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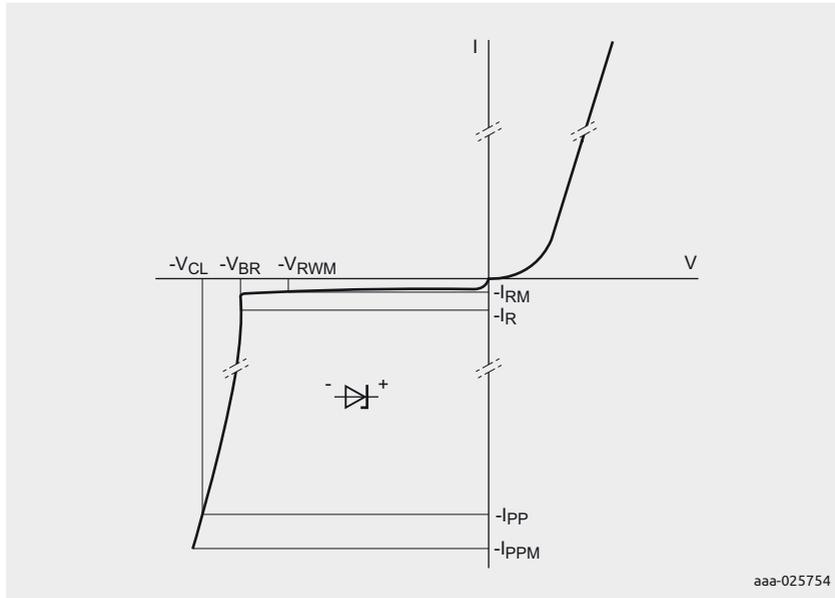
Figure 17 | I-V curve of a Zener-diode or avalanche type ESD protection diode

4.3 Bidirectional ESD protection with Zener diodes

If two Zener diodes with opposite directions are connected in a series, as shown in Figure 18, a bidirectional ESD device is created. If the two diodes are identical, the I-V curve is symmetrical, as depicted in Figure 19.

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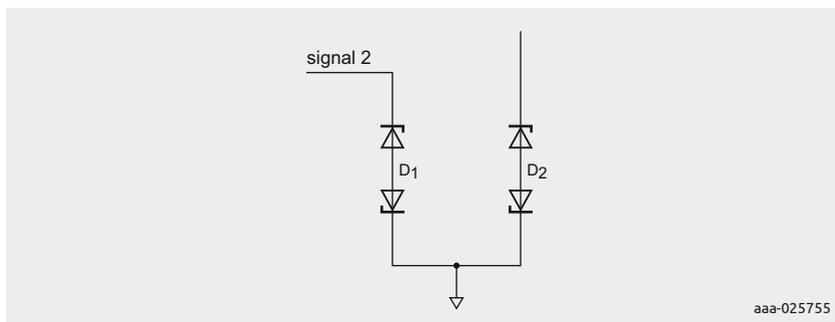
Figure 18 | ESD protection with a bidirectional ESD protection diode.

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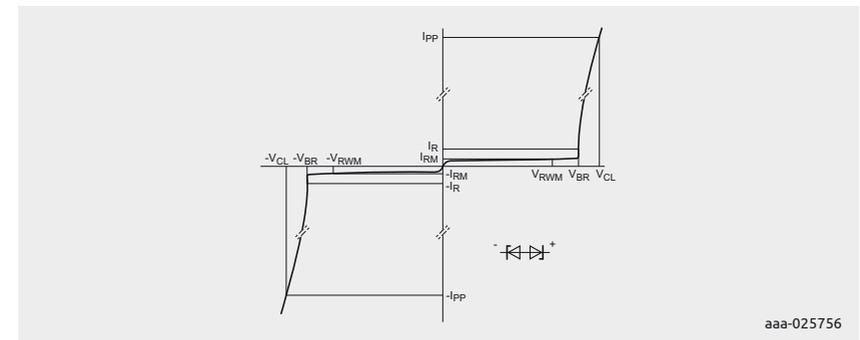
Figure 19 | I-V curve of a bidirectional ESD diode with a simple avalanche behavior

The calculation of the clamping voltage is the same as the equation for the reverse direction of unidirectional ESD diodes:

$$V_{CL} = V_{BR} + I_{PP} \cdot R_{dyn} \text{, with } V_{BR} = V_{BR1} + V_F$$

The V_F value is adding a portion to V_{BR} and the reverse breakdown V_{BR1} of the other diode. Bidirectional ESD protection has to be applied to interfaces that operate with positive and negative voltage ranges. For example, analog audio signals. Most digital interfaces that only operate with positive voltages can be protected with a unidirectional solution. Anyhow, many designers make use of bidirectional ESD protection. The SOC are exposed to much higher negative clamping voltages for negative ESD strikes. This should be avoided if possible because it can badly affect the system level robustness.

This problem is particularly relevant if a system chip has to be protected against negative surge events with higher energy and longer pulse duration, as specified in the IEC 61000-4-5 standard. If the surge protection addresses only ESD pulses according to IEC 61000-4-2, a relatively insensitive chip might be sufficiently protected with a bidirectional topology.

When designing low capacitance ESD protection components it can be helpful to choose this structure with two ESD diodes in series because the parasitic capacitance is lower compared to a unidirectional device, as the below commonly known equation shows:

$$C_d = \frac{C_1 \cdot C_2}{C_1 + C_2}$$

Another reason for choosing bidirectional ESD diodes is that the mounting direction is not important.

4.4 Rail-to-rail topology with pn-diodes and Zener diode

Figure 20 shows an ESD protection environment with a rail-to-rail topology:
- From each signal line, one pn-diode is connected to the upper rail, while another pn-diode is connected from the signal node to the ground rail (GND)
- A Zener diode is connected between ground and upper rail
- Positive surge pulses push the energy through the upper diodes towards the upper rail
- Negative surge pulses push the energy through the lower diodes towards ground
- To improve the ESD performance, the upper rail can be connected to the supply voltage

The Zener diode functions as a clamping device and limits the voltage of positive surge events. If the upper rail is connected to a supply line or Vbus, current can flow into the supply as well where, typically, capacitors can damp incoming pulses. As a negative side effect, microcontroller circuits can show soft fails generated by the supply voltage overshoot created.

The rail-to-rail structure allows a very robust structure with a high capacitance of the Zener diode. The pn-diodes are comparatively small, with a small parasitic capacitance. C_d on the signal line is roughly twice the capacitance of the pn-diode, assuming that the top and ground rail works like a short circuit for RF components. This short is caused by the Zener diode's big capacitance and the comparatively big capacitors connected to the supply line.

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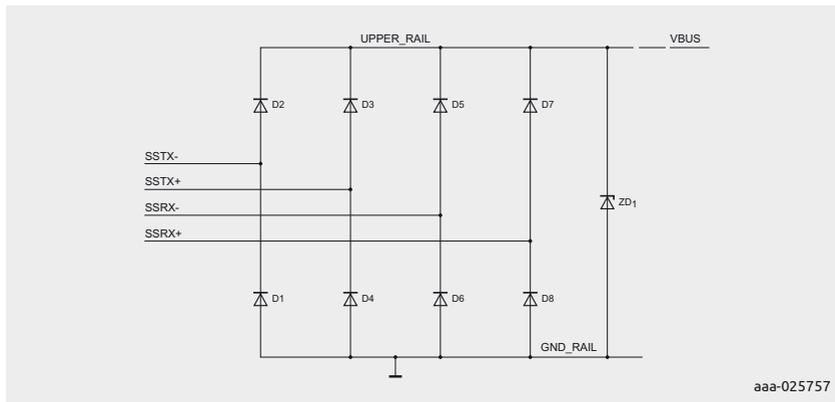
Figure 20 | ESD protection with rail-to-rail topology

4.5 Rail-to-rail topology with SCR

Figure 21 contains a modification of the conventional rail-to-rail topology. Instead of a Zener diode, an silicon-controlled rectifier (SCR) is put between upper rail and ground. If the voltage of the upper rail exceeds a specified trigger voltage, the SCR switches into on-state and connects the two rails. If the current through SCR falls below a specified hold current, the SCR switches off again and becomes high-ohmic again.

Please note that when this protection topology is used, a supply line cannot be connected to the upper rail or to the signal inputs. In the case of a trigger event, the SCR would not return into the off-state because a DC-supply can easily provide a constant current above the hold current I_{hold}. The ESD protection component could be damaged or the supply line stays in a short-circuit condition.

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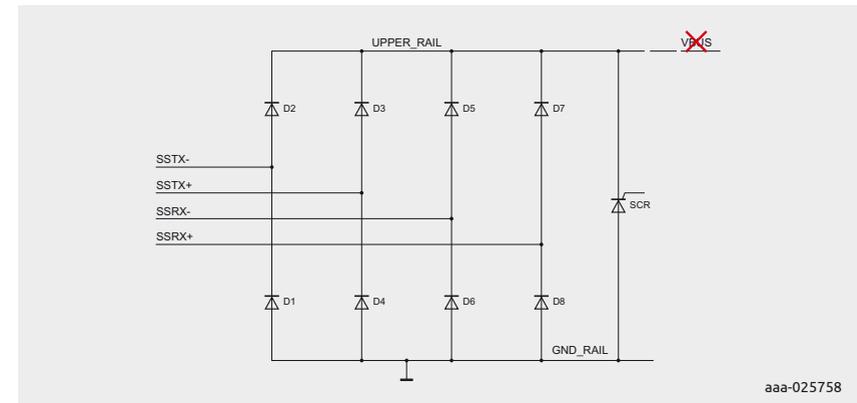
Figure 21 | Rail-to-Rail ESD protection device with SCR

The advantage of the SCR-based approach is that very low clamping voltages can be achieved for surge events. The turn-on effect is often called snap-back because the voltage at the ESD protection device jumps down from a trigger voltage towards a low voltage in on-state. The snap-back voltage can be designed to drop lower than the high state voltage of a signal line and below V_{RWM}. Although this appears to be a conflict, in most cases it does not create a problem. Many high-speed interfaces are designed to be free of DC content in the data stream. Therefore, the data lines do not stay in single-ended high-state. Once the signal toggles back to low-state the hold current or hold voltage condition for the SCR is violated and the ESD component switches off again.

Beside testing with a suitable I-V curve tracer, the snap-back characteristic can best be evaluated with a TLP test. Figure 22 shows a TLP curve of PESD3V3Z1BSF as an example for a TrEOS snap-back device. The device triggers at about 9 V and snaps back to 2.5 V. From there the TLP I-V-graph shows a mostly linear curve with a steepness of $R_{dyn} = 0.19\,\Omega$.

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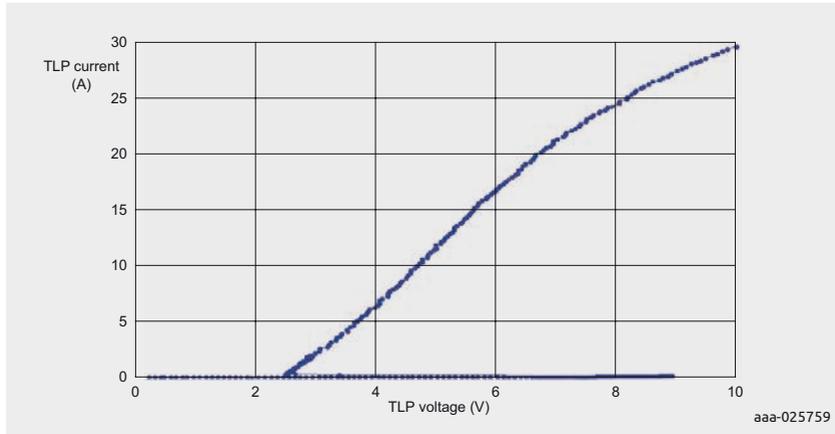
Figure 22 | TLP-Curve example of PESD3V3Z1BSF

Figure 23 compares typical TLP curves with each other, as described below.

- **Green TLP curve:** ESD protection products that are based on an avalanche effect clamping topology that are specified for operating with V_{RWM} 5 V to 5.5 V. They have a breakdown voltage V_{BR} that is equal to or greater than 7 V.

- **Red TLP curve:** Parts that are specified for operating below or equal V_{RWM} 3.3 V have a lower breakdown voltage of typically equal or greater than 5 V. Thus, clamping voltages are lower and more current of the surge event is dissipated in the protection device compared to the 5 V type.

- **Yellow TLP curve:** TLP testing can also be applied to interface pins and complete electronic products. Modern ICs often show TLP curves that start at relatively low voltages. As soon as the pulse voltage is raised, they show a steep increase of current, which is due to a low dynamic interface resistance.
  Please note that many ICs can only cope with a relatively low maximum TLP current. This can be $I_{PP} = 5\,A$, for instance.

- **Black TLP curve:** Shows a deep snap-back topology example. By adding an SCR, very low clamping voltages after turn-on of the device can be realized. A big portion of the surge energy is dissipated in the ESD protection and the overall system level robustness is improved. The destruction voltage of the yellow curve is reached for much higher currents.

In conclusion, effective ESD protection requires a TLP curve for the ESD protection device that is located left of the TLP curve of the SoC. The curve must show a high steepness with no cross point to the SoC curve. In this way it can be ensured that most of the surge current flows through the protection; and only a lower current through the IC input structure. The point where the system is destroyed is shifted to higher currents. An ideal TLP curve would be perpendicular ($R_{dyn} = 0\,\Omega$), where the clamping voltage does not increase with the surge current.

With an avalanche topology, the breakdown voltage cannot be decreased any further down into the operating voltage range of the interface without causing leakages. This means that further improvement for a low clamping voltage can be driven in the direction of a perpendicular TLP curve only. However, dynamic resistance decrease has technological limits. Therefore snap-back topology allows lowest clamping voltages and highest system protection levels for sensitive interfaces.

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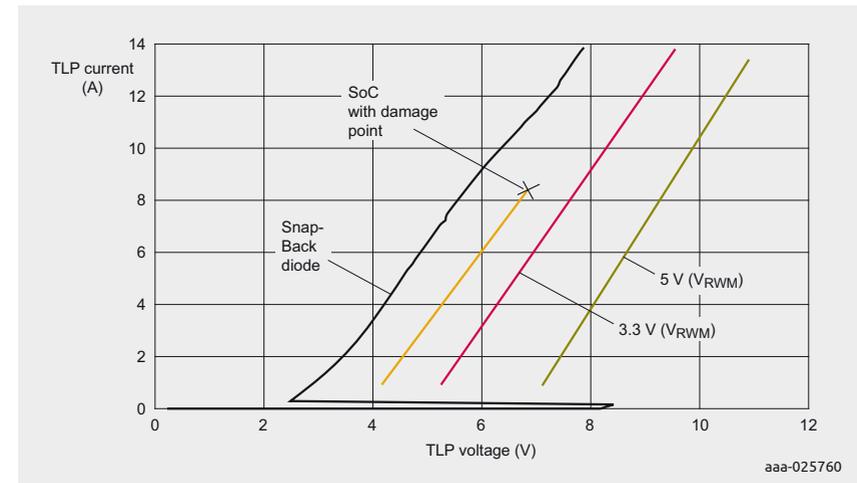
Figure 23 | TLP-Curves of avalanche type ESD diodes with VRWM 5 V (green), Vrwm 3.3 V (red), SoC (yellow with point of destruction) and snap-back ESD diode

4.5.1 Example: Intel Z77 IC-HUB and PUSB3FR4

Figure 24 compares two ESD protection scenarios. TLP is measured at the input pins of a test PCB. The magenta curve shows the TLP curve of an Intel Z77 IC-Hub RX input, while the cyan TLP curve shows the same device with PUSB3FR4 as ESD protection:

- The magenta TLP curve shows a relatively high dynamic impedance of around 3 Ω. The SoC manages up to 3.5 A pulse current.

- The cyan TLP curve shows the characteristics achieved with the 4-line PUSB3FR4 protection device. The curve shows an I-V characteristic with a deep snap-back and a steep linear line after the ESD protection device has triggered. Most of the surge current flows via the PUSB3FR4 and not into the SoC. This is achieved due to a very low dynamic resistance, which is only one tenth of the system chip resistance. Thus, most of the surge energy is dissipated in the protection device. The system chip is therefore protected very effectively, with an excellent level of system robustness. An extremely high TLP current would be required again to reach the TLP voltage for destruction for the SoC (about 9.5 V).

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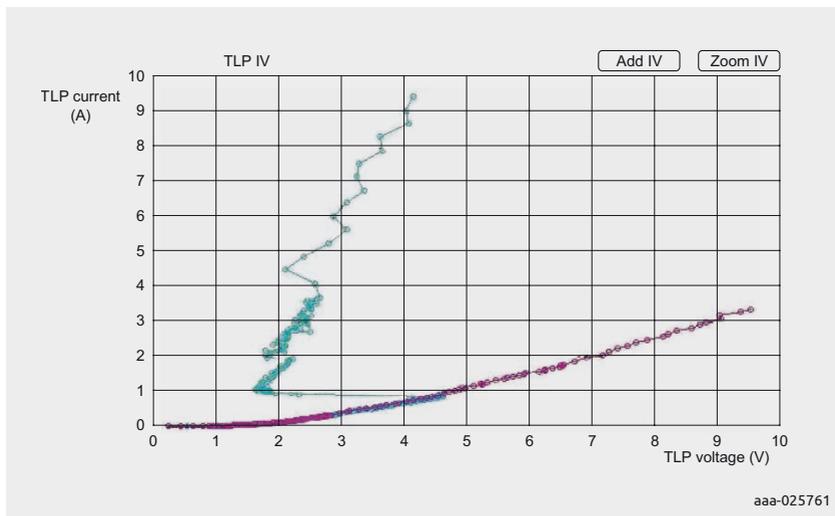
Figure 24 | TLP-Curve Rx line Intel ICH BD82Z77 stand-alone (magenta) and combined with PUSB3FR4 (cyan)

4.5.2 Latch-up scenarios

If a snap-back device is triggered, a latch-up can happen if the on-state current is higher than the hold current of the ESD protection device. However, most ESD protection devices withstand the current arising from this condition: Nexperia parts were tested in latch-up with 100 mA for several hours without showing any damage or degradation. If an interface is affected, a soft fail occurs but no hardware fail. For many interfaces, the snap-back device automatically returns to its off-state once the affected data line is in single-ended low state.

An HDMI interface requires some attention with respect to possible latch-up conditions. The HDMI interface topology is given in Figure 80. Many HDMI input circuits are designed with active silicon circuits for the 50 Ω pull-up resistors. HDMI interfaces have to be safe for short-circuits on the TMDS lines according to HDMI standard requirements. To avoid overheating of active pull-up resistors, the pull-up voltage is shortly removed whenever a short is detected at the TMDS lines. This mechanism releases a latch-up condition.

Please note that Transmission Minimized Differential Signal (TMDS) lines begin data transfer after connection is established. The risk of ESD strikes is much higher during the connecting process of a cable, and very unlikely to happen at a cable with fully established connection. In practice, no known field returns are caused by latch-up failures with HDMI interfaces.

The maximum latch-up current for HDMI can be calculated in a straightforward way. The pull-up voltage can be 3.5 V (3.3 V + 5%) as maximum and the pull-up resistors can have a minimum resistance of 45 Ω (50 Ω −10%). Assuming a snap-back voltage of 1.24 V, the maximum potential latch-up current can be calculated as 50 mA. If the hold current of the ESD protection is smaller than this value, there is a potential risk for the interface to hang-up. More Details on HDMI interfaces can be found in Chapter 8.

I²C bus interface is another example that can be affected by latch-up conditions. The maximum high-state current of this interface is defined by the selected pull-up resistors. There is no potential problem if the high-state current is lower than the hold current of the ESD protection device. If it is higher, the I²C-bus master detects the hang-up situation on the bus and can initiate a power cycle to release the bus again.

4.5.3 Analyzing load lines to judge the risk of latch-up scenarios

Figure 25 shows an I-V characteristic of an interface output driver with a detailed I-V diagram of a snap-back ESD device.

The load line of an interface starts at a short circuit current on the y-axis. It shows a linear decay toward the open circuit case where the x-axis is crossed at the data line drive voltage V_{DD}.

The ESD protection I-V curve shows a hysteresis. The arrows mark which trace is valid for the direction of test voltage change. If the voltage increases, the snap-back triggers as soon as the trigger voltage is reached. From that point onwards, the curve continues on a steep on-state path. When the testing current is decreased below I_{hold}, the ESD protection device turns off again, utilizing the lower paths, shown in the diagram, to leap to higher voltage. In similar scenarios as shown in the diagram, an ESD strike can produce a latch-up condition. An interface can get stuck at operating point 1. To be safe from a latch-up scenario, the load line of an interface should only cross the I-V curve of the protection device once.
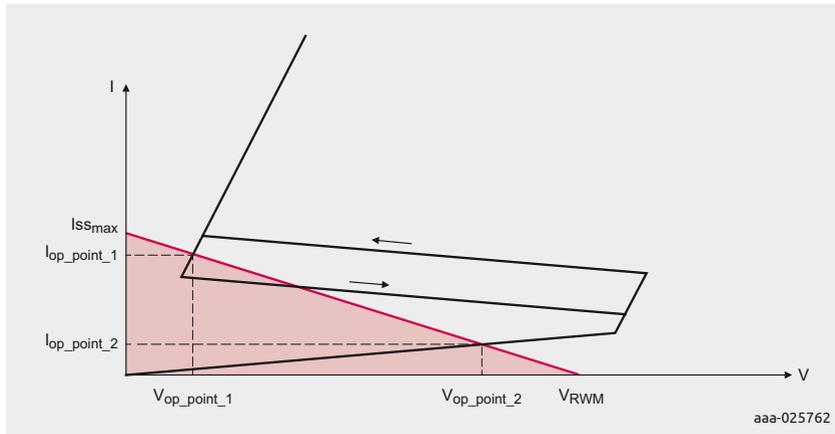
Figure 25 | I-V characteristic of interface output driver; snap-back ESD protection device

In an established USB Type-C connection (pin assignment Table 17), the configuration channels CC1 or CC2 are connected to V_{conn}. V_{conn} is a 5 V DC supply. Sideband usage signals SBU1 and SBU2 can be overlaid by a DC. This applies to analog audio use cases in which the DC supplies amplifiers. A snap-back ESD diode that can snap below a DC level of a signal line should not be selected for these cases. Of course, V_{Bus} is suitable for snap-back devices in this context.

4.5.4 Hold current and hold voltage of TrEOS protection devices

In Figure 26 the I-V curve shows measurement results with a current-driven curve tracer for the unidirectional TrEOS product PESD5V0C1USF. The curve delivers a hold current of I_{hold} 16 mA and a hold voltage of V_{hold} 1.4 V. A hysteresis curve can be seen, as explained in the previous section. I_{hold} and V_{hold} can be derived from the current and voltage point at the lower left corner of the hysteresis area.
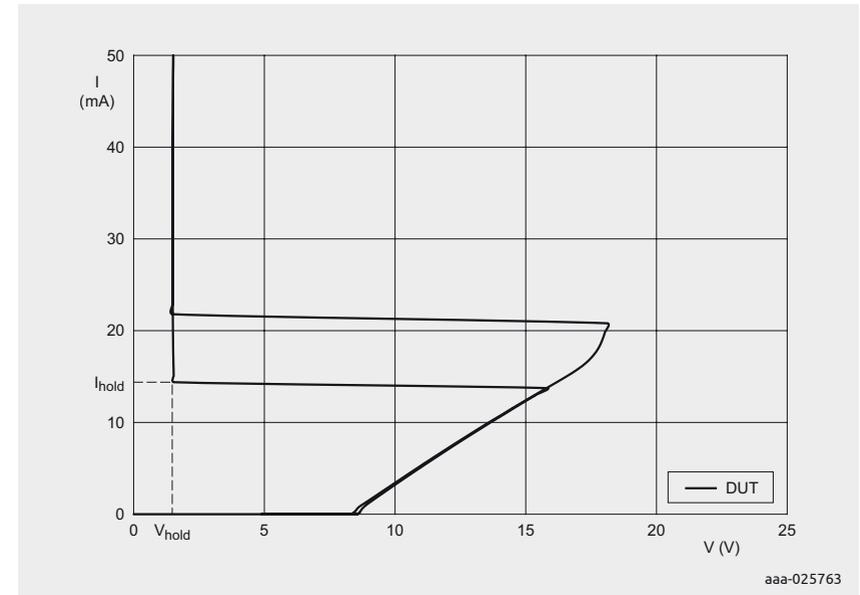
Figure 26 | I-V curve of unidirectional PESD5V0C1USF with hysteresis characteristic

The I-V curve of Figure 27 shows measurement results with a current-driven curve tracer for the bidirectional TrEOS product PESD5V0H1BSF. The curve delivers the same hold current as for the unidirectional part, which is I_{hold} +/− 16 mA. The hold voltage is ±V_{hold} 2.2 V. The hold voltage V_H is higher because of the bidirectional solution's series structure, which also includes an additional V_F value of 0.8 V of a diode that is driven in forward direction.
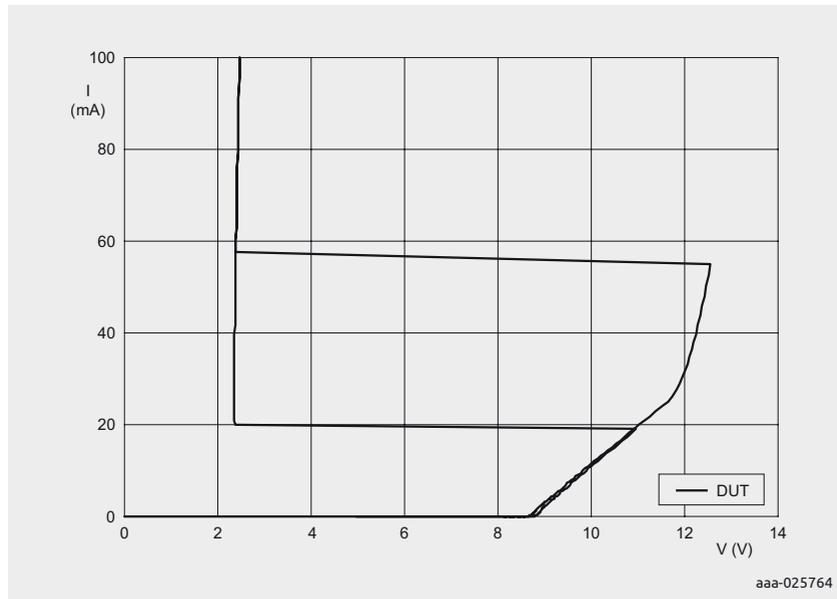
Figure 27 | I-V curve of PESD5V0H1BSF with hysteresis characteristic

4.5.5 Switching speed of snap-back ESD protection

An effective ESD protection limits a surge pulse to a safe clamped voltage within a short time without excessive and wide overshoots. This temporal behavior, as shown in Figure 28, can be evaluated with a VF-TLP test by analyzing the voltage traces of the single test events.

Figure 28 shows a voltage and current trace of a VF-TLP test for a PESD5V0H1BSF at a peak current I_{PP} of 15 A, with pulse width 5 ns, and rise and fall time of 600 ps. The voltage trace shows a narrow overshoot. After device turn-on, the comparatively low clamping voltage is reached [34].
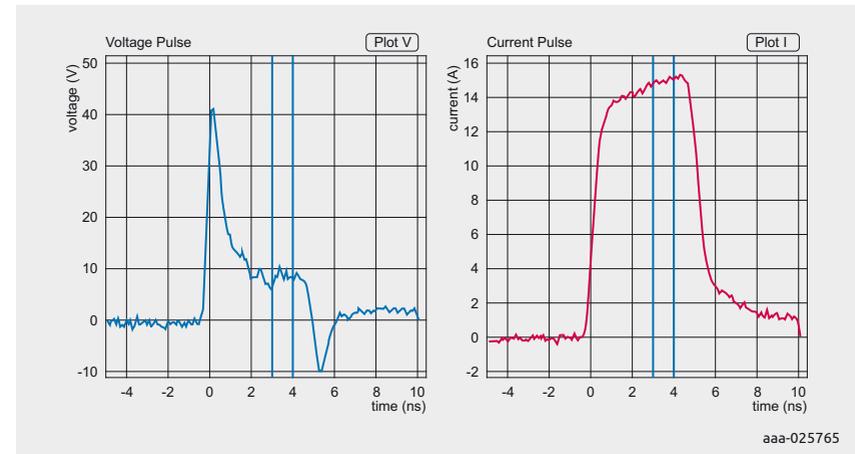
Figure 28 | VF-TLP (5 ns/200 ps) voltage and current traces PESD3V3Z1BSF at I_{PP} = 15 A

Figure 29 shows a way how the turn-on time can be derived from a VF-TLP voltage scope trace. The average value in the 70% to 90% window is taken as zero percent reference value for the falling edge. The TrEOS devices turns on within approximately 1 ns, as Figure 28 shows. The switching time interval is derived from the 30% values at the rising and falling edges of the voltage overshoot in the scope trace.

For many products in the market, the turn-on time is relatively long. This prevents the device from switching on at all in a VF-TLP pulse. Turn-on times of about 10 ns are often encountered. Devices that show this weakness cannot protect very sensitive high-speed interfaces and cannot achieve the required system robustness.
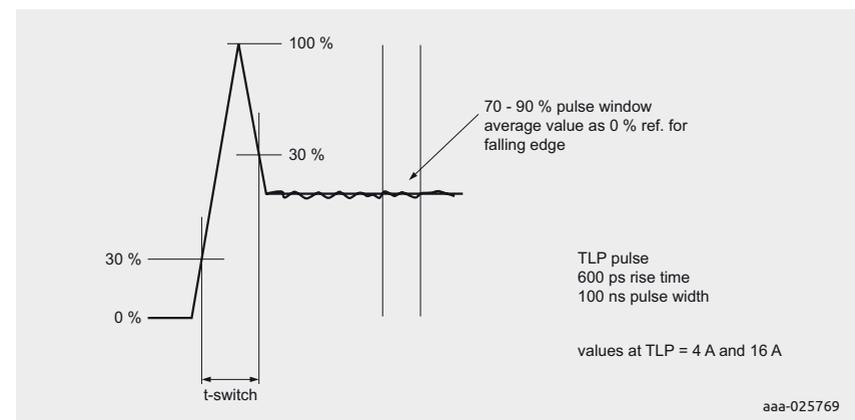
Figure 29 | Measurement of switching time (turn-on time) based on VF-TLP test pulse

4.6 Findings for ultra-high-speed interfaces and SoCs

As stated in Section 3.2, tests with ESD guns have a widespread destruction level, should the first overshoot be critical for the system chip. Tests with HMM, TLP and VF-TLP pulses deliver much more stable and reproducible results.

Figure 30 shows an HMM current trace marking the limit of a sensitive SoC for this kind of test pulse. The IC was tested without an external ESD protection. The peak current of the first overshoot is 2.4 A. The current peak of the second shoulder is 1.8 A. In Figure 31 such a device with VF-TLP pulses is tested. The device is destroyed when 2.4 A as peak current is reached; like in the first overshoot in the HMM test above. The peak voltage for this pulse is 21 V.

In an additional test, as shown in Figure 32, the interface chip is tested with a 100 ns wide TLP pulse. The destruction level is 4.1 A, which is much more than the value of the HMM pulse shoulder. This means the SoC device is damaged by the first overshoot of an ESD strike. Note that the damage does not occur during the shoulder, where the higher amount of energy of the overall surge pulse is located. For the latest generation of ESD-sensitive ICs an effective ESD protection must limit the first overshoot effectively, which is achieved by a fast reaction time and low clamping.

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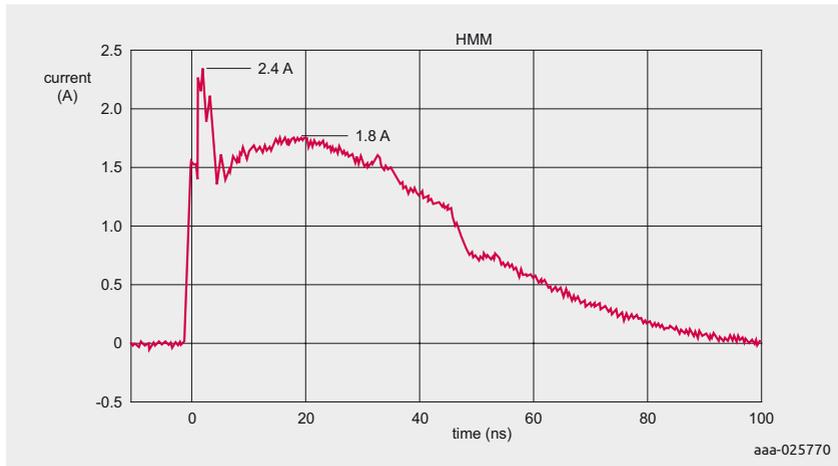
Figure 30 | HMM current curve and fail level for a sensitive 10 Gbit/s USB 3.1 SoC

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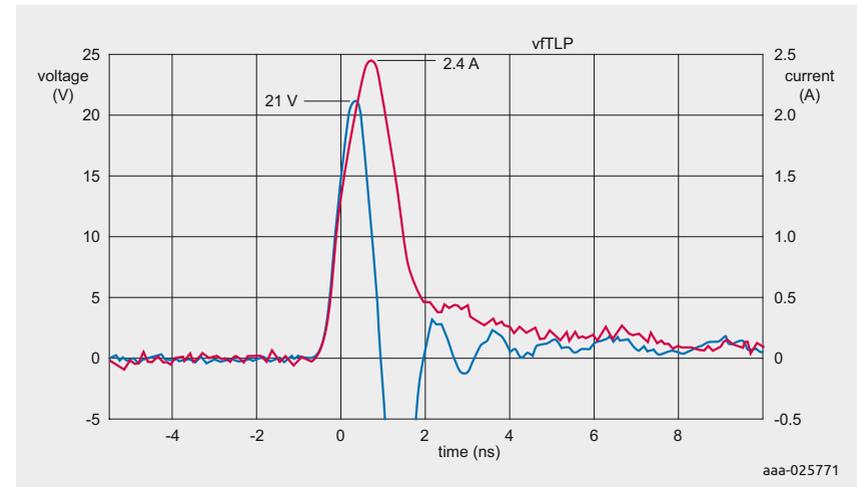
Figure 31 | VF-TLP fail level for this interface

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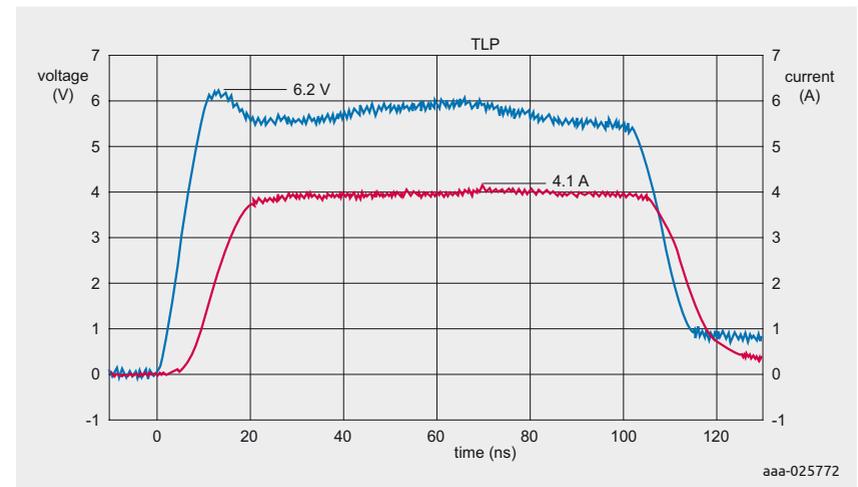
Figure 32 | TLP fail level for this interface

4.7 Effect of parasitic inductance

Figure 33 shows an equivalent circuit for an IC input with an additional external ESD protection that can be used to simulate a surge event:

- The IC has a rail-to-rail ESD protection structure for the input pin.
- The upper diode is connected to a voltage clamping element with an additional serial resistance of RS.
- LS and RB represent the inductances of the IC bond wires or internal connections and the parasitic inductance of the signal routing on the PCB.
- RB is the serial ohmic impedance between interface and IC input.
- The external ESD protection component is represented by a voltage clamping element, a serial resistor Rc and a parasitic capacitance Lc.

In order to achieve effective ESD protection and good system level robustness, it is helpful that Lc is very small in relation to Lb + Ls. This improves the damping of the first overshoot of an ESD strike.

ESD protection components with comparatively long bond wires show a bigger parasitic inductance than components with CSP-like concepts. The DSN0603-2 (SOD962) package has an extremely low parasitic inductance of about 1 nH only. The DFN2510A-10 (SOT1176) package, which is used extensively in computing applications, has an inductance of about 3 nH. With longer traces on the board — I.e. from the connector to the SoC — the inductance of the connection to the IC can be increased. This increase shifts the balance towards a safer region.

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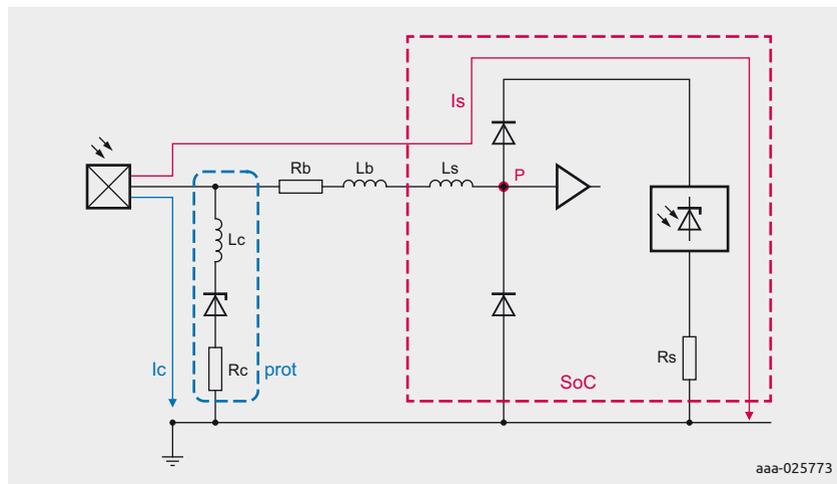
Figure 33 | Equivalent Circuit for an IC input pin with ESD protection

4.8 Layout and placement hints for an effective ESD protection

As a general rule, it is recommended to put the ESD protection devices close to the entry point of ESD and surge events. Normally this is a connector on a board for user interfaces or board to board connections. The current path through the ESD protection needs to be as short as possible to keep parasitic inductance and resistance as low as possible. As depicted in Figure 33 the board has to be designed in a way that most of the surge current takes the path through the ESD protection and not into the system chip. A comparably higher inductance and resistance in the path towards the SoC helps to reduce the surge energy and voltage at the chip to be protected.

Figure 34 shows a USB Type A connector protected by single ESD protection diodes in the package SOD962. Three lanes are protected, RX+/RX-, TX+/TX- and D+/D-. One pin of each diode is connected without stubs to the data line. The other pin is directly connected to ground with shortest possible wires.
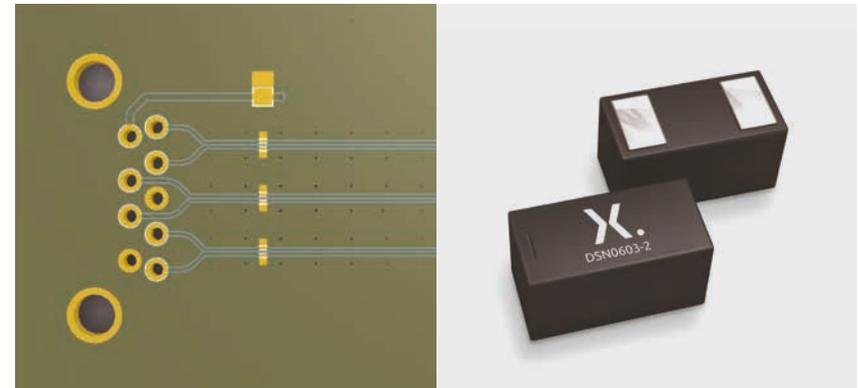
Figure 34 | Layout example with ESD protection diodes in DSN0603-2 (SOD962)

Figure 35 is an example of an ESD protection designed with the multi-line package DFN2510A-10 (SOT1176). For a multiline package, there is less flexibility for the routing compared to single ESD diodes. All signal lines have to go from the connector to the protection device and from there to the system chip.
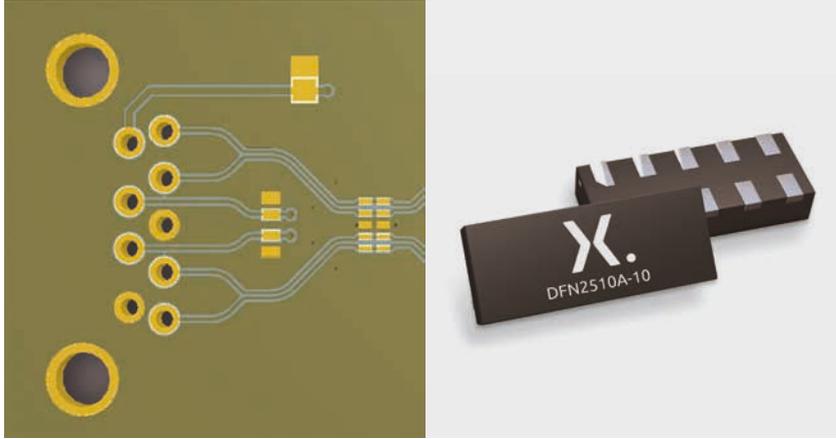
Figure 35 | Layout example with ESD protection diodes in DFN2510A-10 (SOT1176).

Chapter 5

**SEED
(System efficient
ESD design)**

A fundamental problem in ESD design is the need for simulation methods that can predict system level robustness. A general misconception is that system level robustness depends on the robustness of individual components. Rather, it depends on several factors. Namely, the robustness of the weakest system-relevant device (usually the SoC that is to be protected), the protection device's properties, other elements in the signal path, and parasitics arising from the board and mounting wires. The idea of 'system efficient ESD design' is to take all these parameters into account in the form of an equivalent circuit or circuit-like simulation to predict system level robustness [8,9].

The quality of the simulation results depends on two factors: The completeness of the system model and the quality of the individual device model, in particular the model of the protection device. The first part can usually be delivered by an experienced engineer. Board parasitics and other, often not desired, model parameters can be extracted from measurements, rule of thumb calculations, or full-wave simulations.

The challenging part is to obtain a suitable model for the protection device. Some devices can be modeled with a modified diode model. Other devices, with snap-back and hysteresis, can only be approximated with simple diode models. To fully represent such a device, more sophisticated models must be used which are currently subject to investigations and often exceed the capabilities of ordinary SPICE-based circuit simulators.

5.1 Creation of a system model

The term SEED refers to the concept of connecting an equivalent circuit representation of the system, including the SoC, with a model of the protection device to evaluate protection performance. There are different ways to realize the system simulation. Besides SPICE-based simulations, combinations with other simulation tools like Verilog-A and customized models based on network parameter blocks can be used. Here, the focus is on SPICE based simulations. This approach is very powerful but reaches a limit when the device models cannot be represented as an equivalent circuit in a straightforward way. Some simulation tools like ADS[1] offer to import models from other simulation environments like Verilog-A into a SPICE-like simulation workbench. In this sense, the system level simulation can be seen as a SPICE-like circuit simulation, but the internal modeling is no actual SPICE [35].

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1 Keysight's ® Advanced Design System

Independent of the simulation tool used, the frequency rage needs to be determined. Usually a maximum frequency or a minimum time step needs to be set in the simulator. Both have the same meaning and are linked with:

$$t_{min} = \frac{1}{2\pi f_{max}}$$

The maximum frequency to be considered depends on the excitation and effects that are simulated. For high-speed data lines the maximum frequency might be determined by the signal frequency. As a rule of thumb for arbitrary pulse excitation signals, two to five times the bandwidth is taken as the maximum frequency. The bandwidth is usually [10] linked to the rise time with:

$$BW = \frac{0.35}{t_r}$$

Table 5 lists some common excitation pulses with corresponding maximum frequencies. These values are minimum requirements. Highly non-linear effects like snap-backs can increase the maximum frequency even more. It is good practice to use these values as a starting point and increase the frequency to see if the values stay the same, or if higher frequencies need to be considered. Many simulation tools automatically select the frequency or time step. Nevertheless, this is one of the first parameters to check when the results are not as expected.

Table 5: Product overview of automotive ESD protection devices

Excitation pulse	Rise time (ns)	Max. Frequency (GHz)	Min. Time step (ns)
IEC 61000-4-2	0.7	2	0.08
JESD22-A-J114D	10	0.1	1.6
IEC 61000-4-5	8000	0.0002	800
TLP	1	1.5	0.1
VF-TLP	0.3	4	0.04

5.1.1 PCB model

There are three practical ways to derive a model for the PCB. If the actual PCB is available in hardware, measurements can be done. If the geometry and material parameters are known, one could do full-wave simulations or use empirical or analytical models. Alternatively, to get a first impression or if the exact routing is not known, one can use rule-of-thumb formulas.

To obtain the models by measurement, a vector network analyzer is used to generate an S-parameter file. These parameters contain information about reflection and transmission for amplitude and phase at selected frequency points. The highest measured frequency should be at least as high as the maximum frequency considered in the simulation. Furthermore, it is very important to properly select the reference points where the probes are placed. Each probe corresponds to a port in the S-parameter block. One should be at the connector, where the ESD pulse will be injected, one is at the SoC input pin that is affected, and the last port is at the mounting destination of the protection device. If only a two-port vector network analyzer is available, the three-port parameter can be reconstructed [11]. Having the S-parameter in place, it can be imported into the simulation environment and connected to the model of the SoC, the protection device, and other device models if desired. For example, it is sometimes practical to do all measurements directly on the PCB and add an additional model accounting for the connector that is exposed to the ESD pulse.

If measurements are not possible or impractical, one can use models to derive the S-parameters. There are many full-wave or 2.5D solvers available that can be used to obtain the S-parameters from known geometry and material parameters. Alternatively, there are empirical and analytical models that are available. Giving an overview and introduction of existing methods would go beyond the scope of this handbook, so the reader is referred to [7].

Sometimes, it is not necessary or not possible to have a very accurate model of the PCB. Especially when the design is not fixed, it is reasonable to make some educated guess and proceed with rule of thumb formulas. A good first guess is to use a simple RLC representation of a short transmission line, see Figure 36, and estimate the values from rule of thumb calculations as [12,13]:

$$C = l\,\frac{\sqrt{\varepsilon_r}}{cZ_0} \overset{FR4}{\rightarrow} \frac{l}{Z_0}\cdot 7\,\frac{\Omega}{mm}\frac{pF}{mm} \overset{50\,\Omega}{\rightarrow} l\cdot 0.14\,\frac{pF}{mm}$$

$$L = l\,\frac{\sqrt{\varepsilon_r}Z_0}{c} \overset{FR4}{\rightarrow} Z_0 l\cdot 7\,\frac{\Omega}{mm}\frac{pH}{mm} \overset{50\,\Omega}{\rightarrow} l\cdot 0.3\,\frac{pH}{mm}$$
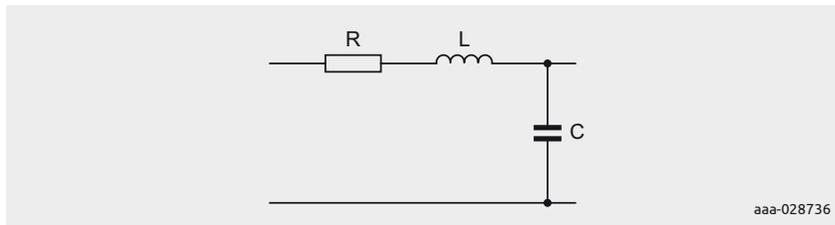
Figure 36 | Equivalent circuit for a short transmission-line

5.1.2 Verilog-A

Verilog-AMS (for Analog Mixed Signal) offers the same facilities as VHDL using a different syntax, but licenses for Verilog-AMS are typically only available in larger electronic or semiconductor companies. Verilog-A (for Analog) uses a reduced instruction set from Verilog-AMS and has the advantage of being available to a broader audience. Verilog-A offers a flexible and simple way to implement diodes and snap-back devices, with and without hysteresis w.r.t. the increase or decrease of the current through the device.

All Verilog-A models presented use a piecewise linear I-V curve. Because the derivative at the inflection points of such a curve is not continuous, convergence problems cannot be avoided completely. One advantage of piecewise linear curves is the ease of calibration. All that is needed to calibrate the model is to enter the measured (V,I) values, measured by TLP (100 ns pulse width and 0.6 ns rise time) for each of the inflection points. No additional optimization of the model is required.

The next sections will treat the available Verilog-A clamp models, as well as the gun and TLP source models, one by one.

5.1.3 Diode Clamp Model
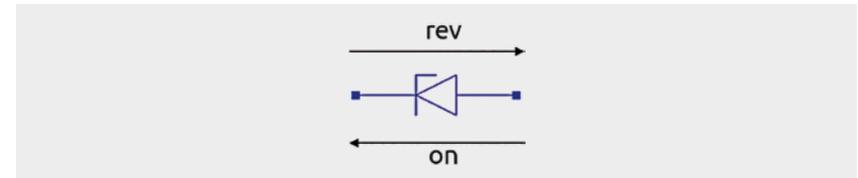
Figure 37 | I-V Diode clamp symbol. The arrows define the 'on' and 'rev' direction of current
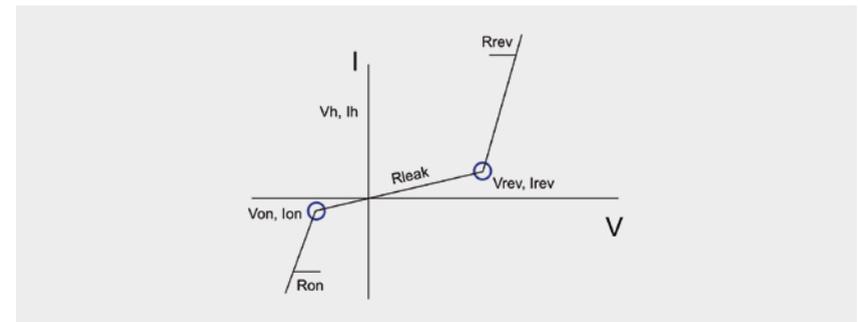
Figure 38 | Piecewise linear I-V curve. The curve is defined by the inflection points [Von, Ion] and [Vrev, Irev] and the slopes for high currents: Ron and Rrev, respectively

The diode clamp model as depicted in Figure 37 is the simplest possible model of a clamp. It basically models a non-ideal diode, which conducts beyond Von in the 'on' direction and Vrev in the 'rev' direction. The series resistance can be specified separately for each direction of current. Note that Rleak has been specified to improve convergence. Typically, a resistance of 1 MΩ is used. The model ignores any snap-back behavior of the clamp. Figure 38 shows an example of a DC sweep of diode clamp.

Despite its simple nature, this clamp model gives a very good prediction of the system's failure level, whether the failure mechanism is thermal damage in either clamp or SoC, or the limiting over-voltage is not reached during protection triggering but at higher currents.

The diode clamp model has the advantage that convergence problems are virtually non-existent. This model provides a very good correlation with measured fail levels, under the restriction mentioned in the previous paragraph.
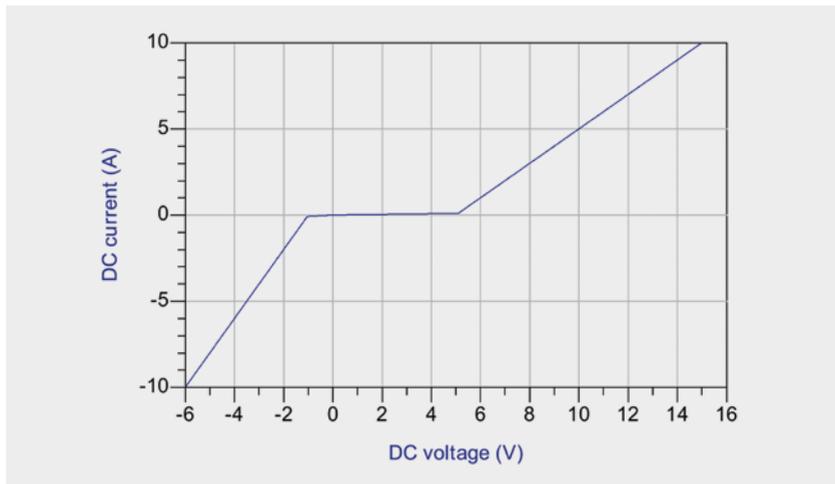
Figure 39 | DC sweep of diode clamp

5.1.4 Clamp model with snap-back

The clamp model with snap-back as shown in Figure 40 is an extension of the diode model, described in the previous section. As depicted in Figure 41, two additional inflection points are defined: [Vt1, It1] and [Vh, Ih]. The clamp triggers at [Vt1 It1] and for I>It1 it will enter its low-impedance state (given by Rrev).
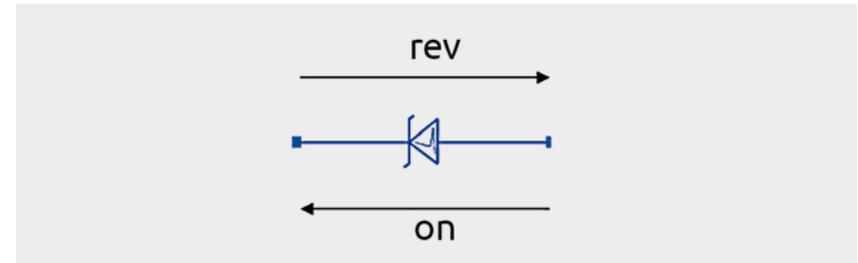
Figure 40 | I-V Diode snap-back clamp symbol. The arrows define the 'on' and 'rev' direction of current
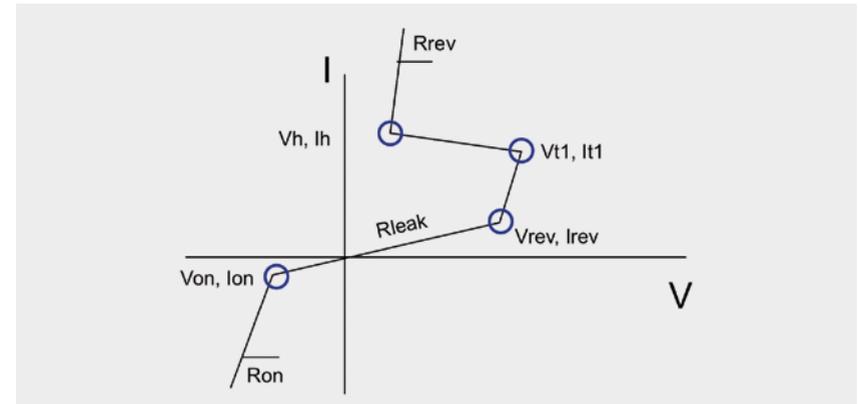
Figure 41 | Piecewise linear I-V curve of snap-back clamp. The curve is defined by the inflection points [Von, Ion], [Vrev, Irev], [Vt1,It1] and [Vh,Ih] and the slopes of high currents: Ron and Rrev, respectively

The minimum voltage and current for this low-impedance state are defined by [Vh,Ih]. Once I<Ih the clamp will return to its high-impedance state. Note that the same curve is traversed when the current is increasing or decreasing (no hysteresis). In other words, the function is single-valued in current. In reality, Ih<It1 always, but the error introduced by the simplification Ih>It1 is small, because both Ih, It1 << It2.

Note further that a distinction has been made between Vrev and Vt1. Vrev is the voltage at which the clamp starts to conduct, which may be due to a trigger device kicking in, e.g. an avalanching junction. Snap-back to the low-impedance state occurs at [Vt1, It1].

Figure 42 and Figure 43 show an example of the modeled internal protection of the TI SN65LVPE502CP USB3 RX I/O. The zoom of the low-current part of the curve shows that all relevant details of the actual I-V curve are captured very well in the snap-back mode.
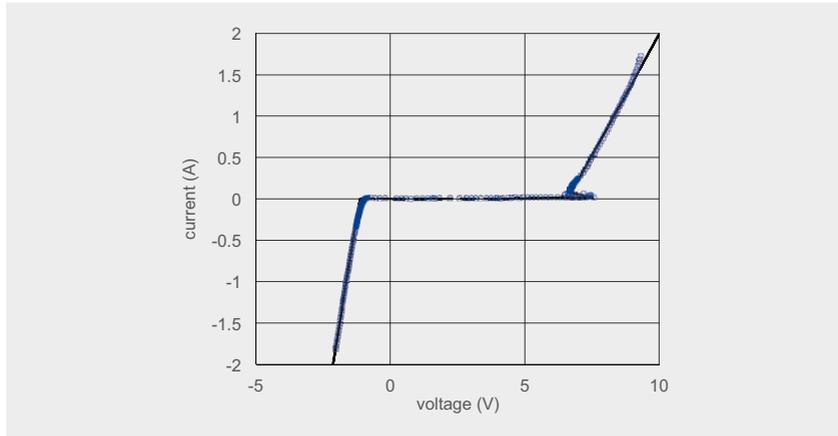
Figure 42 | Modeling [black dashed line) of the TLP measured I-V curve (blue circles) of an internal protection of a TI SN65LVPE502CP USB3 RX I/O
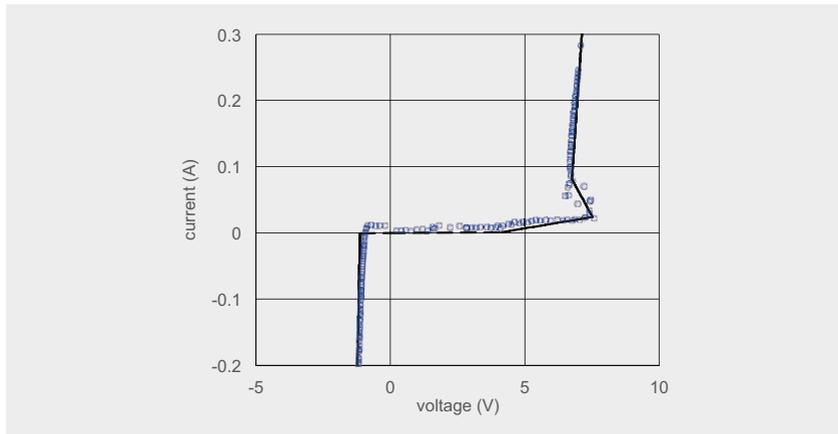
Figure 43 | Zoom of Figure 76 for small currents

5.1.5 Clamp model with snap-back and additional kink

The Verilog-A model allows the model to be extended easily with an additional inflection point (using two additional lines of code. See the appendix for the difference in code).
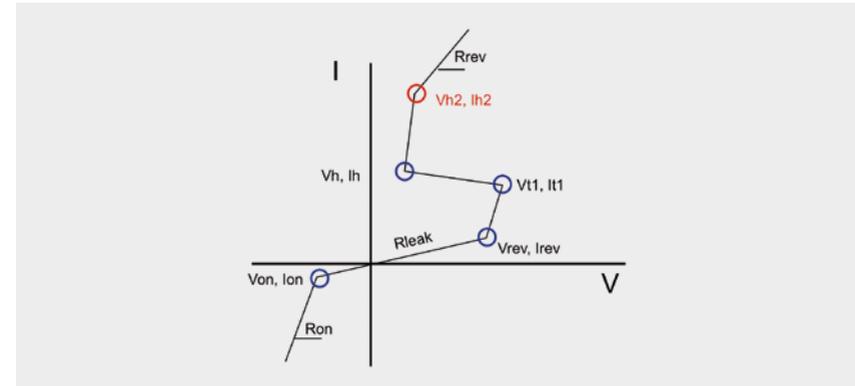
Figure 44 | Piecewise linear I-V curve of snap-back clamp with additional inflection point [Vh2, Ih2].

With this extension, the high-current behavior of the TI USB driver[1] can be modeled more accurately. Figure 45 shows the result with the better match above 1.5 A compared to Figure 42.
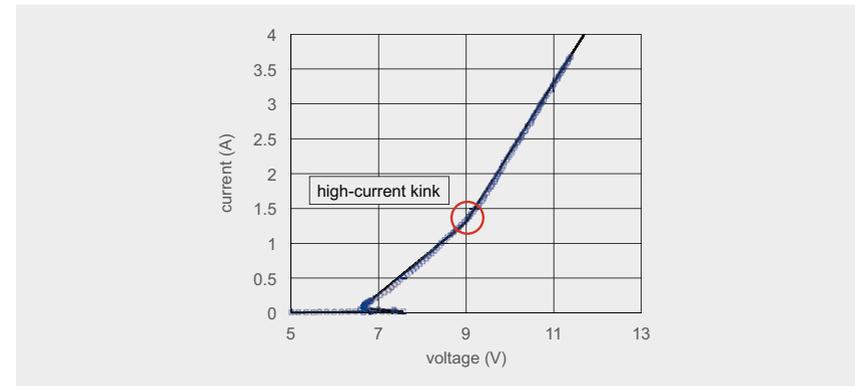
Figure 45 | Modeling (black dashed line) of the TLP measured I-V curve (blue circles) of an internal protection of a TI SN65LVPE502CP USB3 RX I/O with an extra kink at 1.5 A

1 SN65LVPE502CP

5.1.6 Clamp model with snap-back and current hysteresis

In the Verilog-A models so far, no distinction is made between increasing and decreasing current. This may lead to unwanted extra overshoots at the end of a pulse as Figure 46 shows.

Due to missing current hysteresis, an additional overshoot appears at the end of a simulated TLP pulse. This does not appear in the measurements, because the lifetime of the carriers injected in the device is much longer than the TLP timescale.
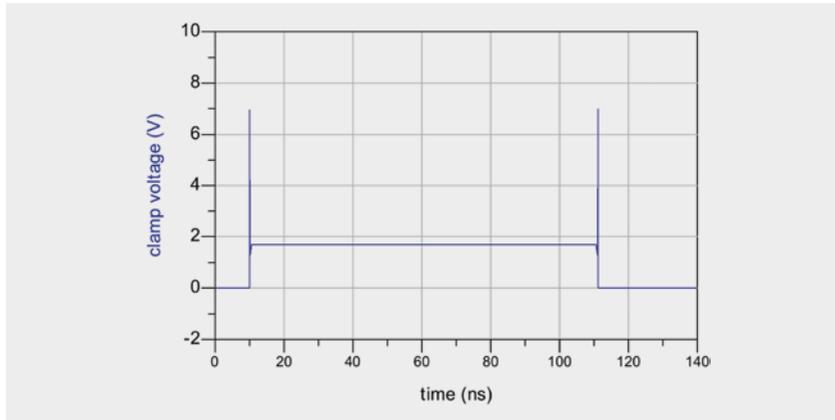
Figure 46 | Unwanted overshoots because of missing hysteresis in model

To suppress such unwanted overshoots, an extended Verilog-A model was created that distinguishes between increasing and decreasing current using the Verilog-A cross-function, which remembers the direction of the current change. Figure 47 depicts an I-V curve of snap-back clamp with hysteresis in current. For increasing current, the black curve is followed, for decreasing current the red dotted curve.
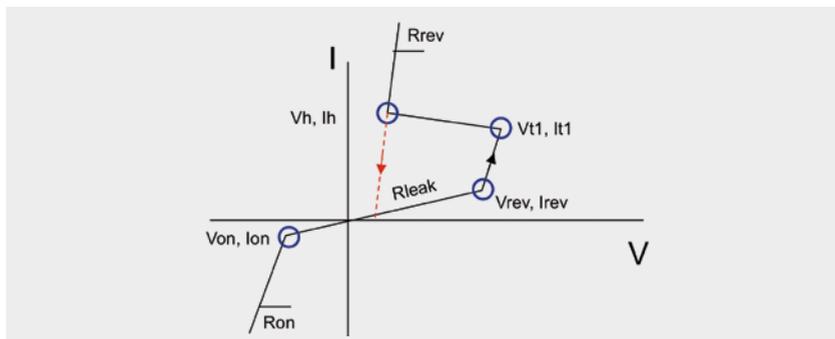
Figure 47 | Piecewise linear I-V curve of snap-back clamp with hysteresis in current.

In Figure 48 the result of the hysteresis model is shown. It no longer contains the undesired overshoot at the end of the TLP pulse.
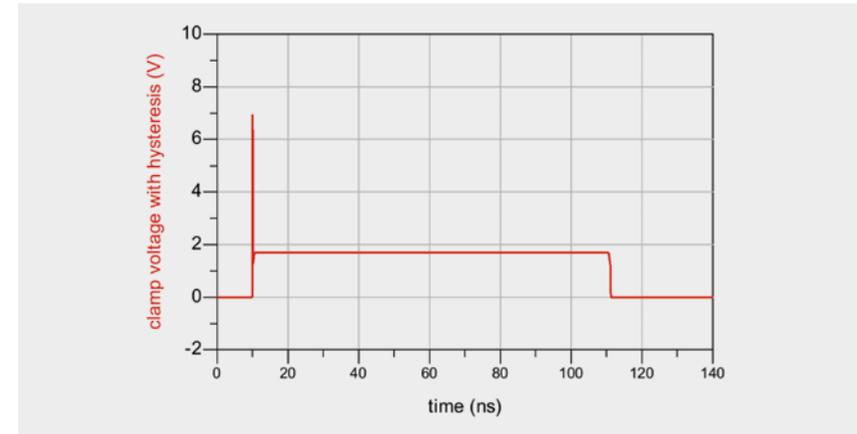
Figure 48 | 100ns TLP pulse modeled with hysteresis model

5.1.7 Dynamic voltage overshoot during triggering

The dynamic voltage overshoot during triggering of the external protection is not included in the Verilog-A model. A partially correct model may be provided by adding a small (~2 nH) inductance in series with the protection. This will provide the proper overshoot for higher TLP currents, but it will underestimate the overshoot for lower currents. For lower currents, the dominant factor determining the overshoot is the amount of charge that needs to be injected into the low-ohmic substrate to provide the necessary conductivity modulation.

5.1.8 TLP current source

The most straight forward source is a TLP source based on a current source and 50 Ω impedance. It is important to note that a voltage source will not work, because the simulated curve is multi-valued in voltage. Therefore, the current in the snap-back region would be undefined. The end effect usually is that the snap-back does not turn up in simulations using a voltage source.
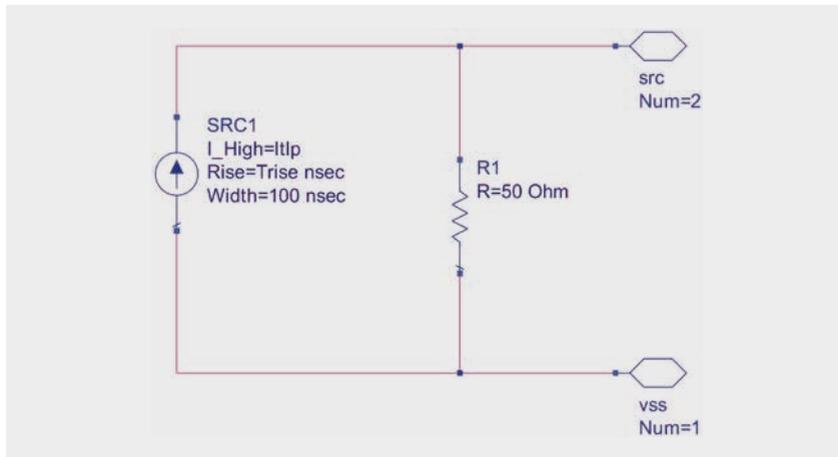
Figure 49 | TLP pulse source based on current source with 50 Ω internal impedance.

5.1.9 TLP IEC 61000-4-2 source (gun model)

The gun model as depicted in Figure 50 is based on the work by Caniggia [14] and Liu [15]. In the idle state switch V3 is closed and C8 is charged. When the pulse is triggered, V3 opens and V2 closes.
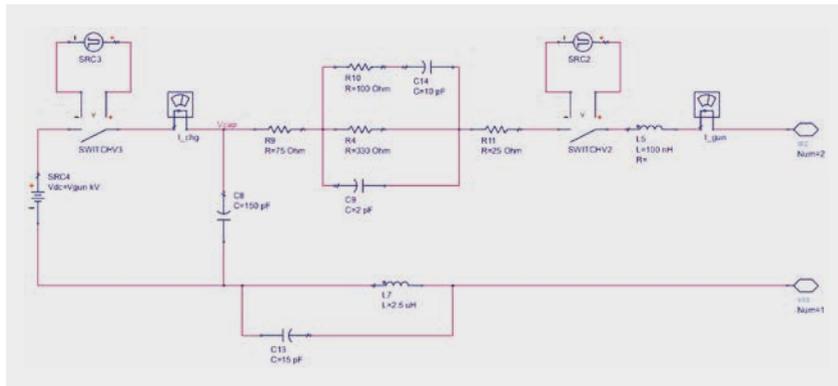
Figure 50 | IEC 61000-4-2 source

As an example, the gun discharge on an application protected by an external protection is simulated. Note that the SoC internal protection (CSB6 in Figure 51) can be simulated by the same Verilog-A model with different parameters.
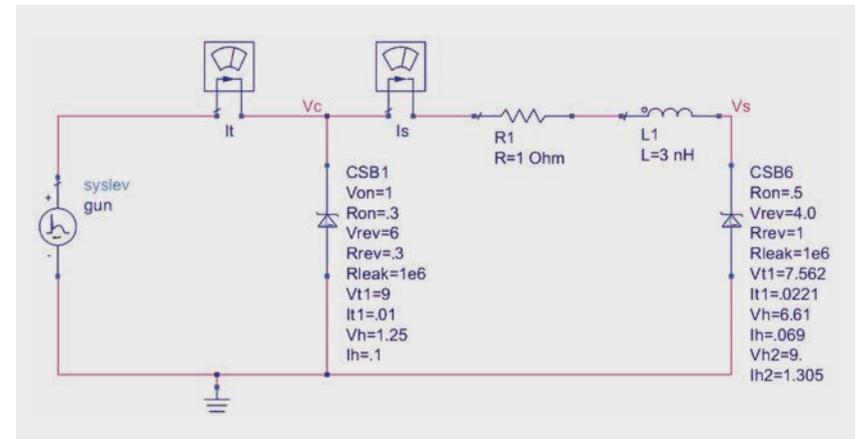
Figure 51 | IEC 61000-4-2 discharge to an application with internal protection CSB6 protected by an external protection CSB1

The results of the simulation are shown in Figure 52 to Figure 54. Note the blue current scale (current into SoC) in Figure 50 is in mA, whereas the red scale (current into external protection) is in A.
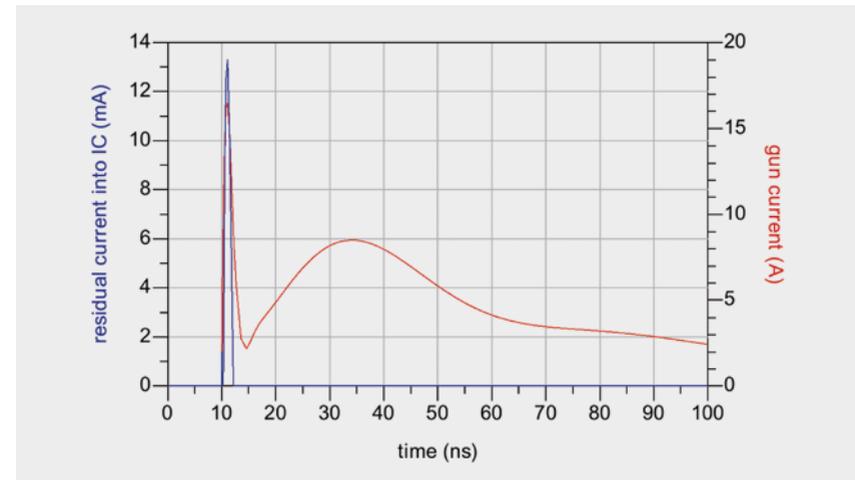
Figure 52 | Simulated current waveforms into the protection (red) and the SoC (blue)61000-4-2 discharge to an application with internal protection CSB6 protected by an external protection CSB1

The current into the SoC for a 4 kV discharge is strongly reduced from 16 A in the first peak to 14 mA as the current waveforms show.

The voltage during triggering is reduced from 6 V to 4 V as depicted in Figure 53 and Figure 54. Using either the SoC fail voltage or fail current, the gun test fail level may be simulated. A detailed example of such a simulation and a comparison with experimental data is given in [16].
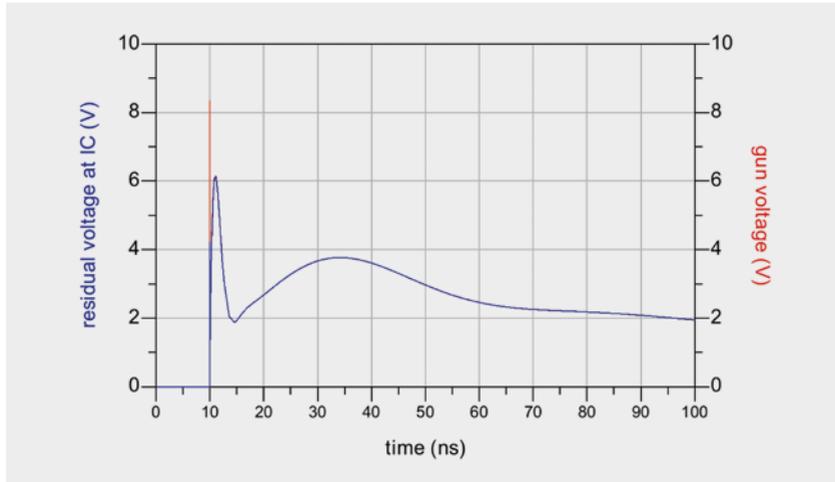
Figure 53 | Simulated voltage waveforms at the protection (red) and at the SoC (blue)
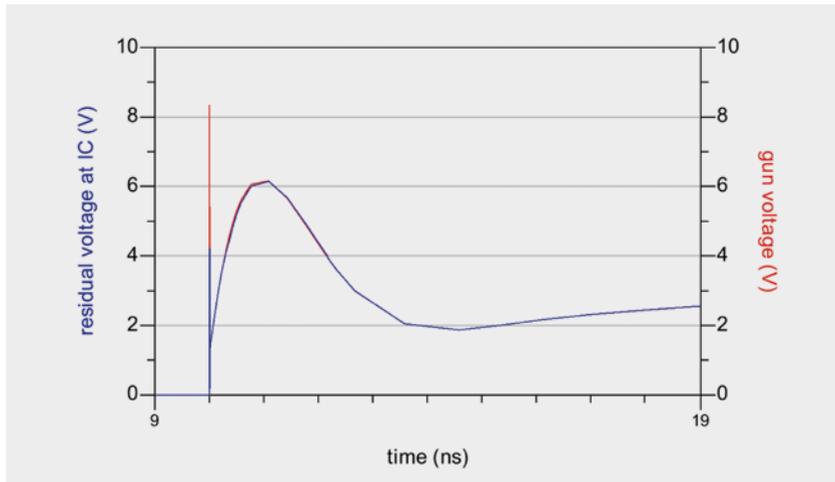
Figure 54 | Zoomed view of the voltage waveform in Figure 50

5.1.10 Verilog-A code examples

Examples of Verilog-A code, below, are provided for the different model characteristics as discussed in the prior chapters. The first example code is for a simple diode clamp, followed by more sophisticated topology with snap-back.

Diode Clamp:

```
// 23-MAY-2013 Guido Notermans
// describes piecewise linear clamp without snap-back

`include "constants.vams"
`include "disciplines.vams"

module clamp(anode, cathode);
  inout cathode; electrical cathode;
  inout anode; electrical anode;
  parameter real Ron=1.0 from (0:inf);
  parameter real Von=1.0 from [0:inf);
  parameter real Rrev=1.0 from (0:inf);
  parameter real Vrev=5.5 from [0:inf);
  parameter real Rleak=1M from (0:inf);
  real Ion; real Irev; real iout; real vin; real vr;
  analog begin vr = -Vrev;
    Ion = Von/Rleak; Irev = vr/Rleak; iout = 0.0;
    vin = V(anode,cathode);
    if (vin<0.0) iout = vin/Rleak;
    if (vin<vr) iout = Irev+(vin-vr)/Rrev; if (vin>0.0) iout = vin/Rleak;
    if (vin>Von) iout = Ion+(vin-Von)/Ron; I(anode,cathode) <+ iout;
  end
endmodule
```

Clamp with snap-back:

```
// 15-JUL-2016 Guido Notermans
// describes piecewise linear clamp with snap-back
`include "constants.vams"
`include "disciplines.vams"

module clamp_sb(cathode, anode);
  inout cathode; electrical cathode;
  inout anode; electrical anode;
  parameter real Ron=0.3 from (0:inf); parameter real Von=1.0 from [0:inf);
  parameter real Rrev=0.3 from (0:inf); parameter real Vrev=5.0 from
[0:inf);
  parameter real Rleak=1M from (0:inf) parameter real Vt1=8 from (0:inf);
  parameter real It1=0.01 from (0:inf); parameter real Vh=1.25 from
(0:inf);
  parameter real Ih=0.1 from (0:inf)
  real Ion; real Irev; real vout; real Iin;
  analog begin
    Ion = -Von/Rleak; Irev = Vrev/Rleak;
    Iin = I(anode,cathode); vout = -Von+(Iin-Ion)*Ron;
    if (Iin>Ion) vout = Iin*Rleak;
    if (Iin>Irev) vout = Vrev + (Iin-Irev)*(Vt1-Vrev)/(It1-Irev);
    //@(cross(Iin-It1,0)) $discontinuity(0);
    if (Iin>It1) vout = Vt1 + (Iin-It1)*(Vh-Vt1)/(Ih-It1);
    if (Iin>Ih) vout = Vh + (Iin-Ih) *Rrev;
    V(anode,cathode) <+ vout;
  end
endmodule
```

Clamp with snap-back:

```
// 15-AUG-2016 Guido Notermans NXP
// describes piecewise linear clamp with snap-back and kink in I-V curve
`include "constants.vams"
`include "disciplines.vams"

module clamp_sb2(cathode, anode);
  inout cathode; electrical cathode;
  inout anode; electrical anode;
  parameter real Ron=0.3 from (0:inf); parameter real Von=1.0 from [0:inf);
  parameter real Rrev=0.3 from (0:inf); parameter real Vrev=5.0 from
[0:inf);
  parameter real Rleak=1M from (0:inf); parameter real Vt1=8 from (0:inf);
  parameter real It1=0.01 from (0:inf); parameter real Vh=1.25 from
(0:inf);
  parameter real Ih=0.1 from (0:inf); parameter real Vh2=2 from (0:inf);
  parameter real Ih2=0.2 from (0:inf);
  real Ion; real Irev; real vout; real Iin;
  analog begin
    Ion = -Von/Rleak; Irev = Vrev/Rleak;
    Iin = I(anode,cathode); vout = -Von+(Iin-Ion)*Ron;
    if (Iin>Ion) vout = Iin*Rleak;
    if (Iin>Irev) vout = Vrev + (Iin-Irev)*(Vt1-Vrev)/(It1-Irev);
    //@(cross(Iin-It1,0)) $discontinuity(0);
    if (Iin>It1) vout = Vt1 + (Iin-It1)*(Vh-Vt1)/(Ih-It1);
    if (Iin>Ih) vout = Vh + (Iin-Ih) *(Vh2-Vh)/(Ih2-Ih);
    if (Iin>Ih2) vout = Vh2 + (Iin-Ih2) * Rrev;
    V(anode,cathode) <+ vout;
  end
endmodule
```

Clamp with snap-back and additional inflection point:

```
// 10-NOV-2016 Guido Notermans
// describes piecewise linear clamp with snap-back and hysteresis

`include "constants.vams"
`include "disciplines.vams"
module clamp_sb_hyst(cathode, anode);
  inout cathode; electrical cathode;
  inout anode; electrical anode;

  parameter real Ron=0.3 from (0:inf);
  parameter real Von=1.0 from [0:inf);
  parameter real Rrev=0.3 from (0:inf);
  parameter real Vrev=5.0 from [0:inf);
  parameter real Rleak=1M from (0:inf);
  parameter real Vt1=8 from (0:inf);
  parameter real It1=0.01 from (0:inf);
  parameter real Vh=1.25 from (0:inf);
  parameter real Ih=0.1 from (0:inf);
  real Ion; real Irev; real vout; real Iin;
  integer state;
  analog begin
    @(initial_step) begin
      state  = 1;
      Ion    = -Von/Rleak;
      Irev   = Vrev/Rleak;
    end
    Iin    = I(anode,cathode);
    @(cross(Iin-Irev,1)) state=1;
    @(cross(Iin-Ih,-1)) state=-1;
    vout   = -Von+(Iin-Ion)*Ron;
    if (Iin>Ion) vout = Iin*Rleak;
    if (state>0) begin
      if (Iin>Irev)  vout = Vrev + (Iin-Irev)*(Vt1-Vrev)/(It1-Irev);
      if (Iin>It1)   vout = Vt1 + (Iin-It1)*(Vh-Vt1)/(Ih-It1);
    end
    if (state<0) begin
      if (Iin>Irev)  vout = Vh  + (Iin-Ih) *Rrev;
    end
    if (Iin>Ih)    vout = Vh  + (Iin-Ih) *Rrev;
    V(anode,cathode) <+ vout;
  end
endmodule
```

Chapter 6

EMI filtering with common mode filters

6.1 Introduction to common mode filters

A common mode filter, often called common mode choke and abbreviated CMF or CMC, consists of two coupled coils. If current flows in the same direction in both coils, the filter has a high impedance. If the currents flow in opposite direction, the impedance is low.

If a common mode filter is applied to a differential data line, the differential part of the data carrying the information can pass. At the same time, the overlaid common signal content is blocked, as depicted in Figure 55. Common mode noise can be generated from non perfect transmitters where the single signal lines are not exactly inverse to each other. Common mode content can easily be created in the PCB layout if a signal pair changes direction and the length of the signal lines is not equal. This effect is depicted in Figure 56.

Magnetic and electrical fields are cancelled out for a differential signal in the far field, if the single signals are routed within a small distance. In contrast, common mode signals can radiate into the environment. Especially in compact designs, like smartphones or smart watches, EMI can reduce the sensitivity of receiver blocks. For example, an activated USB 3.0 interface can hinder proper reception of WiFi data.
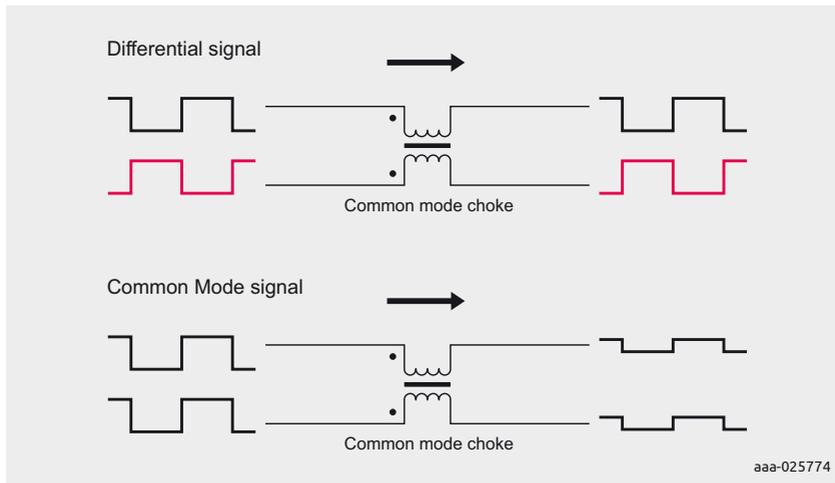
Figure 55 | Common mode choke signal with differential and common mode input
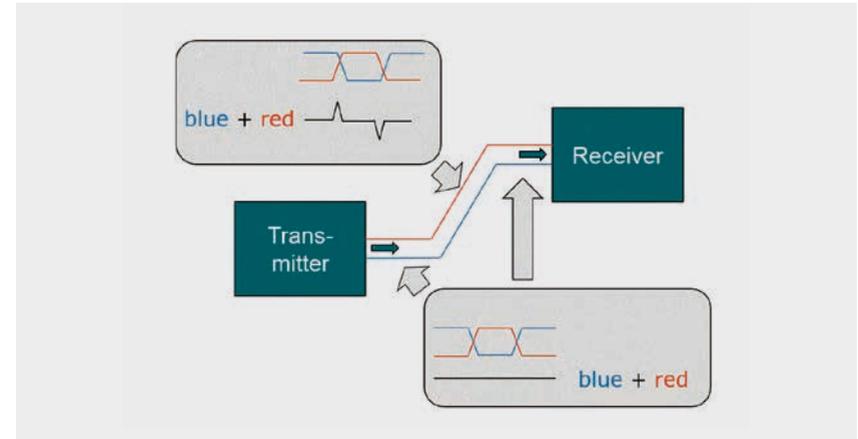
Figure 56 | Common mode Noise from Routing

Figure 57 shows an overview of the frequency bands of RF transmission standards for mobile devices with red markers at 2.5 GHz and 5 GHz. 2.5 GHz is the fundamental wave of USB 3 generation 1. 5 GHz is the fundamental wave of USB 3 generation 2.

Please note that 2.5 GHz EMI components create EMI problems for some WiFi, LTE and Bluetooth bands. In some scenarios the use of common mode filters prevents loss of the WiFi connection while a USB 3.0 interface is active. Consequently, this eliminates the need to force down the USB data speed from super speed to high speed.
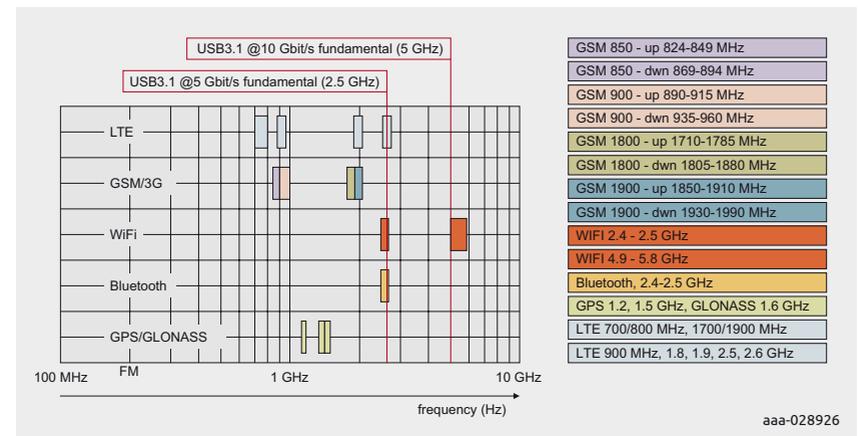
Figure 57 | Frequency bands of important RF transmission standards

6.2 Common mode filters combined with ESD protection

Usually ferrite-based common mode filters are combined with stand-alone ESD protection devices. Silicon device manufacturers have designed CMFs with copper windings deposited on a silicon die including ESD protection. The over air coupled coils do not suffer from saturation effects like to be expected for ferrite cores.

The advantages of an integrated CMF together with ESD protection are a reduction of the overall mounting space on the PCB and the prevention of additional impedance drops in the signal traces, which are quite likely at each of the separate parts.

Devices protecting one, two or three lanes are available. This allows maximum board design flexibility, depending on designer preferences. The common mode filter and ESD protection combination is also available as stand-alone ESD protection with the same packages.

These parts are especially helpful for designers considering whether an EMI filter is needed or not at a later stage. In conventional designs in parallel to the footprint for a common mode filter, footprints for two resistors are applied. When a common mode filter is not used, the two resistors are still required to bridge the input and output of the filter. However when designing in the CMF and ESD protection combination these resistors are not required, as the stand-alone ESD protection versions provide this through-connection, simplifying overall design and assembly.

6.3 Differential passband

Selecting a CMF, it has to be ensured that the fundamental wave of a differential data signal passes the filter with low losses. Figure 58 shows the differential passband of the PCMFxUSB3B as an example. The $-3\,dB$ bandwidth is 6 GHz. The attenuation for 2.5 GHz, which is the fundamental wave of USB 3.0 Gen 1 (5 GHz/s), is about $-1.5\,dB$. For USB 3.0 Gen 2 (10 Gbit/s), the corresponding value at 5 Ghz is about $-2.5\,dB$.
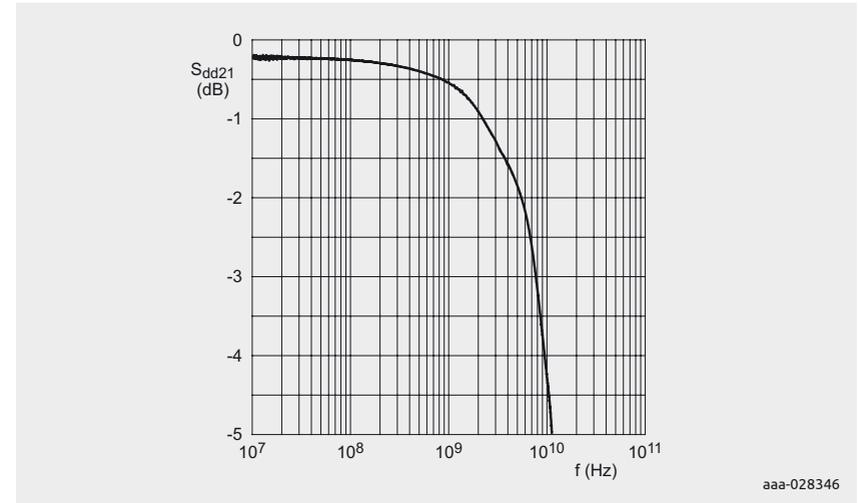
Figure 58 | Differential mode insertion loss curve (S_{21dd}) for PCMFxUSB3B, typical values

It is not correct to compare the frequency response curves of the PCMFxUSB3B with the combined common mode filter and ESD protection to a standalone common mode filter. Such a comparison would disregard the deterioration of the passband caused by the separate ESD protection. Consequently, the passband of the complete circuit of a common mode filter and ESD protection must be compared to the PCMF solution.

To highlight this in more detail, the following example is given. A ferrite filter with $-3\,dB$ bandwidth of 6.3 GHz is combined with an ultra-low capacitance ESD protection device.

Figure 59 shows the S_{21DD} curves for a high runner ferrite-based common mode filter for USB 3, and the combination with ESD protection diodes with different passbands of 7 GHz and 14 GHz.

The black curve represents the stand-alone common mode filter with $-3\,dB$ bandwidth of 6.3 GHz. The red curve shows the CMF combined with a 14 GHz ESD protection device. The overall bandwidth is reduced to 4.9 GHz. With the blue curve the CMF combined with a 7 GHz ESD protection device is depicted. The yellow $-3\,dB$ line is crossed at 4 GHz already. A fundamental wave at 5 GHz is damped significantly.
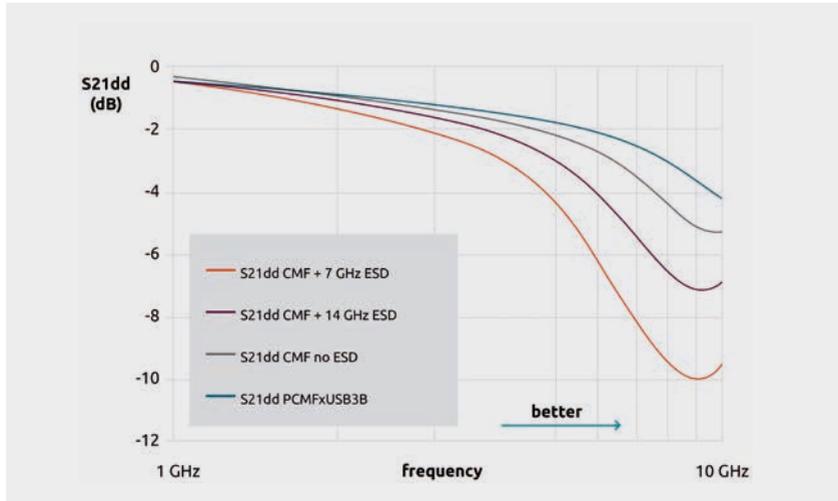
Figure 59 | Overall insertion losses S$_{21dd}$ for a stand-alone common mode filter and different ESD protection devices

6.4 Common mode rejection

An ideal CMF would have a high common mode rejection (S$_{21cc}$) regardless of frequency applied. Practical devices work efficiently in a limited frequency band.

Figure 60 shows the common mode rejection frequency curve of the PCMFxUSB3B. The transfer curve shows a notch at 2.5 GHz down to about −40 dB. Power is attenuated by 4 magnitudes and potential common mode noise of a 5 Gbit/s data signal can be blocked very effectively. In customer-designed applications the benefit of the PCMFxUSB3B shows its particular strength. Especially concerning the maximum WiFi reception distance, which is achieved regardless of an active USB 3 data interface.
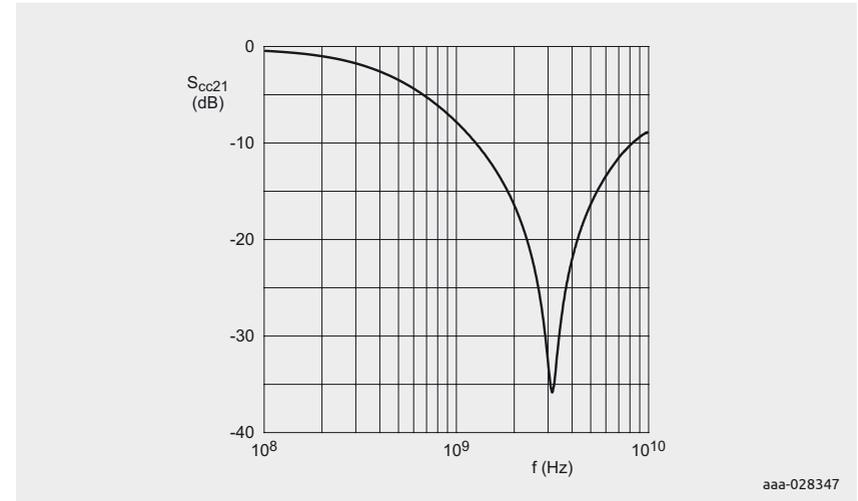
Figure 60 | Common mode rejection curve for PCMFxUSB3B, typical values

6.5 ESD protection performance of combined CMF and ESD protection

The approach of putting a CMF into a data line provides very good protection for sensitive SoCs. As stated before regarding Figure 36, a common mode filter creates a comparably high inductance towards an SoC input.

Measurement test and simulation test results correspond very well, as shown in Figure 61. Measurement results for the residual first peak voltage at the SoC input are shown in solid lines. Simulated results are presented in dotted lines for an ESD protection in wire-bonded package as red curve (DFN1006-2), a flat package without bond wires (DSN0603) as blue curve, and a common mode filter in wafer-level chip scale package (WL-CSP) as green curve.

The DSN and WL-CSP packages have no bond wires, and this is why they have very low peak voltages because of their extremely low parasitic inductance of about 5 nH. Current through the protection path can increase very fast so that low current flows into the system chip to be protected. As the green curve shows, the inductance of the common mode filter improves the result even more. The curves that are measured look very similar to simulated results concerning the peak voltages.
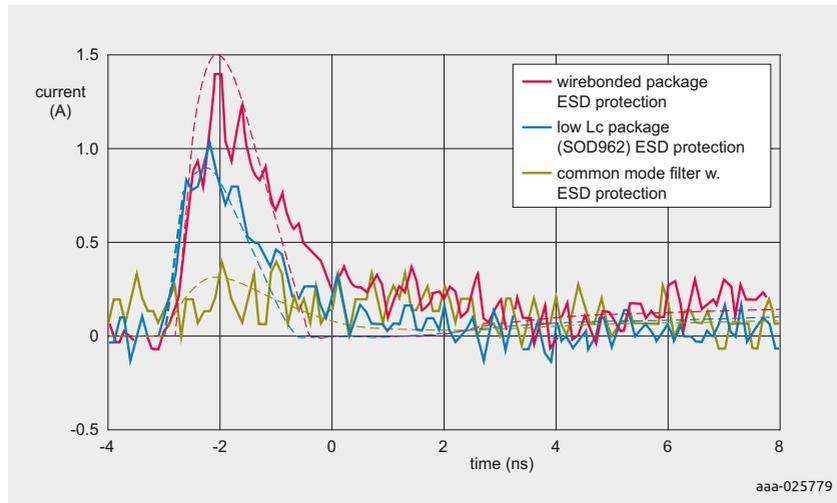
Figure 61 | Residual first peak voltage at the SoC input [16]

The combined CMF and ESD protection devices are typically placed close to the connectors on the PCB. The ESD protection diodes face in the direction of the connectors, as shown in Figure 62 for the example of PCMFxUSB3B in WL-CSP 5 package. In this way the ESD protection works most effectively. However, sometimes it is useful to deviate from this rule and put the common mode filter close to a transmitter stage, if common mode signal content is generated there. In this case, additional care is necessary to avoid generating common mode signal content in the routing path behind the filters.
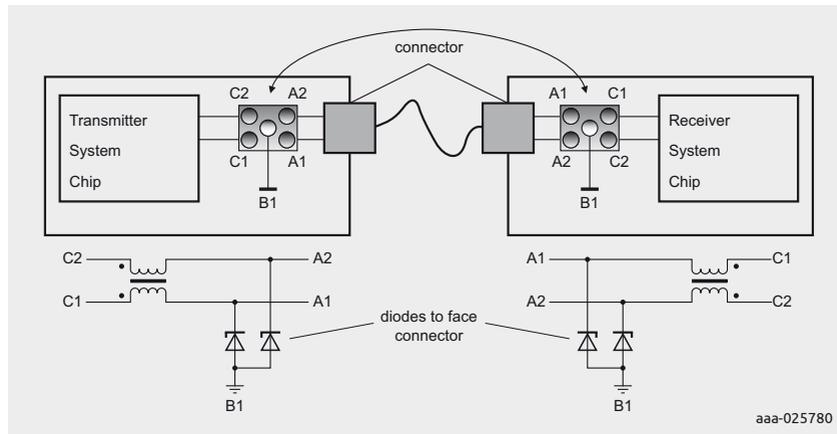
Figure 62 | Orientation of PCMFxUSB3B

Chapter 7

Failure Symptoms in electronic components caused by ESD and surge events

In case electronic devices have been destroyed, silicon chips or electronic components are often analyzed if visible failure symptoms like burn marks can be found. The nature of the destructive event shall be found out from such inspection. It shall be concluded if damage was caused by an ESD strike , by a more massive surge event or by excessive thermal stress above the specified limits. For this kind of classification it is worthwhile to have a brief comparison of most important key parameters of standardized surge signals.

Table 6 lists these key parameters of different surge testing standards in a direct comparison. IEC 61000-4-2 events have a very short rise time, peak current is high with 30 A for an 8 kV ESD gun strike. Anyhow pulse energy is not very high with about 16 µJoule. Human Body Model (HBM) [17] pulses carry even less energy and show lower peak current and slower rise time. 8/20 µs test pulses have about 3 decades more energy compared because of the long pulse duration and low surge generator output resistance. 100 ns TLP pulses are in a similar league in terms of pulse energy and rise times like IEC 61000-4-2 pulses, whereas very fast TLP is even lower in energy. A pulse with a peak current of 15 A corresponds to about 3.5 mJoule.

Figure 63 shows a good example of ESD damage at an IC die. The damaged area is very small, nonetheless insulating layers and gate oxide can be degraded and destroyed. Leakage current can lead to functional fail. Figure 64 gives another example of ESD damage. It shows a tiny hole burnt into the crystal as a visible result of the surge event.
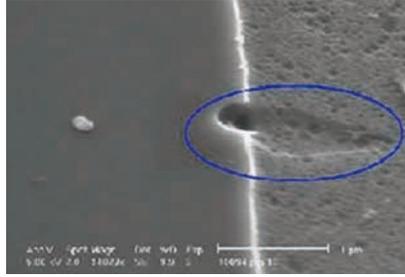
Figure 63 | ESD damage with small burn mark

Figure 64 | Example of ESD damage

Table 6: Comparison of surge standards

Parameter	8kV System level ESD (IEC 61000-4-2) [3]	8kV Chip level ESD HBM (JESD22-A-J114D) [17]	Short Circuit Surge (8/20µs) (IEC 61000-4-5) [2]	TLP [4,5]	Very fast TLP (VF-TLP) [6]
Rise time	1 ns	10 ns	8 µs	1 ns	300 ps
Pulse length	not specified (>100 ns)	not specified (>400 ns)	28 µs	100 ns	5 ns
Peak current	~30 A @8 kV (1 ns) ~16 A @8 kV (30 ns)	~6 A @ 8 kV (10 ns) ~2.2 A @ 8 kV (160 ns)	up to 2000 A	up to 80 A	up to 80 A
Peak Power	~3000 W (30 A,100 V)	~120 W (6 A,20 V)	~250 W (15 A,16 V)	~200 W (25 A, 8 V)	~200 W (25 A, 8 V)
Average Power	~160 W (16 A,10 V)	~22 W (2.2 A,10 V)	~125 W (7.5 A,16 V)	~200 W (25 A, 8 V)	~200 W (25 A, 8 V)
Pulse Energy	**~16 µJoule**	~8.8 µJoule	**~3.5 mJoule**	~20 µJoule	~1 µJoule
Pulse Shape					
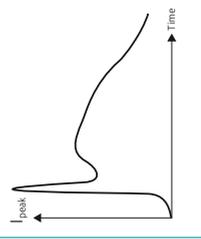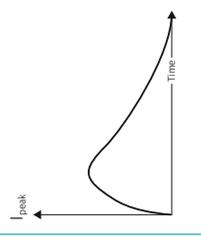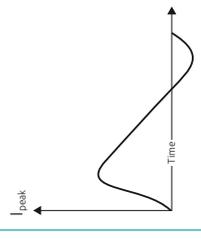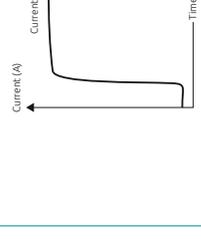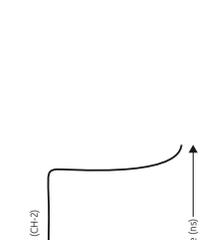
The damage shown in Figure 65 shows a burn mark created by an IEC 61000-4-5 robustness test. The die of a logic buffer was exposed to an 8/20 µs surge pulse from a generator programmed to 42 V charging voltage. The peak current of this test can be assumed to be roughly 20 A with the 2 Ω output resistance of the generator used. The burned area is bigger compared to an ESD strike; metal connections are fully burnt away.

Figure 66 is an example of an EOS (Electrical Overstress Event). Such damage results from thermal overstress where limiting values for power dissipation or maximum current of a device have not been obeyed. The damages on the crystal are severe and the burnt area is relatively big. Sometimes packages are cracked and carbonized with EOS damages. In the case of high currents, fused bond wires are very often observed.
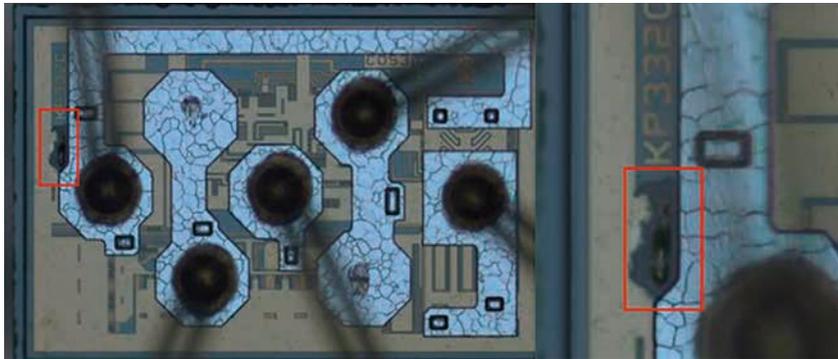
Figure 65 | IEC 61000-4-5 surge pulse damage (8/20 µs surge with 42V generator set-up)
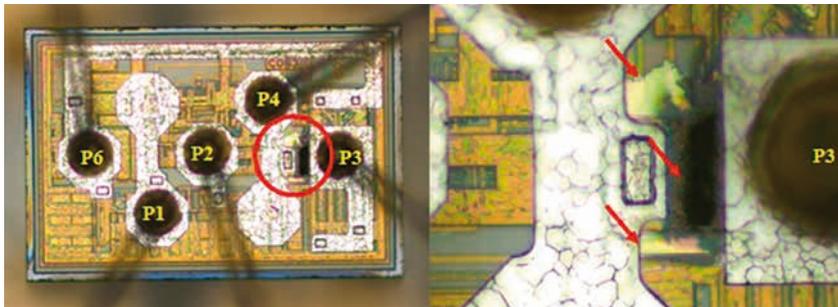
Figure 66 | Electrical overstress damage example (EOS)

Chapter 8
Interfaces & applications

8.1 USB standards, data speeds and coding methods

8.1.1 USB 1.0 and USB 2.0 interfaces

Table 7 shows an overview of contemporary USB standards and their related symbol rates.

Table 7: Overview of data rates for USB interfaces

USB Type	Speed class	Data Rate	Symbol rate (Baud rate) Coding method
USB 1.0	Low Speed (LS)	1.5 Mbit/s = 187.5 kByte/s	1.5 MByte/s NRZI-Code with Bit-Stuffing
USB 1.0	Full Speed (FS)	12 Mbit/s = 1.5 Mbit/s	12 Mbit/s NRZI-Code with Bit-Stuffing
USB 2.0	High Speed (HS)	480 Mbit/s = 60 MByte/s	480 Mbit/s NRZI-Code with Bit-Stuffing
USB 3.0	Super Speed	4000 Mbit/s = 500 MByte/s	5000 Mbit/s 8b10b-Code
USB 3.1	Super Speed +	9697 Mbit/s = 1212 MByte/s	10000 Mbit/s 128b132b-Code
USB 3.2	Super Speed +	2 lane operation with Type-C connector operation; doubling of effective data rate	

USB 1.0 and USB 2.0 use a non-return-to-zero-inverted (NRZI) coding. Typically, NRZI coding, which is also referred to as NRZ coding, follows a simple rule:

state 0: toggle | state 1: constant

When this method is applied, the polarity of a connecting wire pair in a cable has no impact on the bit sequence. This is an advantage because a change in polarity represents a 0 state, regardless of the transition direction. Figure 67 shows the schematic of the logic required for the hardware implementation of an NRZI encoder. The input signal is fed to an inverted input of an Exclusive-Or (XOR) gate. The XOR gate is a digital logic gate that gives a true (1 or high state) output whenever exactly one of the inputs has a 1-state. If both inputs are 1, or both are 0, the output equals false (0 or low state).

Behind the XOR gate, a flip-flop samples the output of the gate by the system clock. The output of the flip-flop represents the output of the coder. It feeds back into the XOR gate; as second input signal for this gate.

aaa-025700
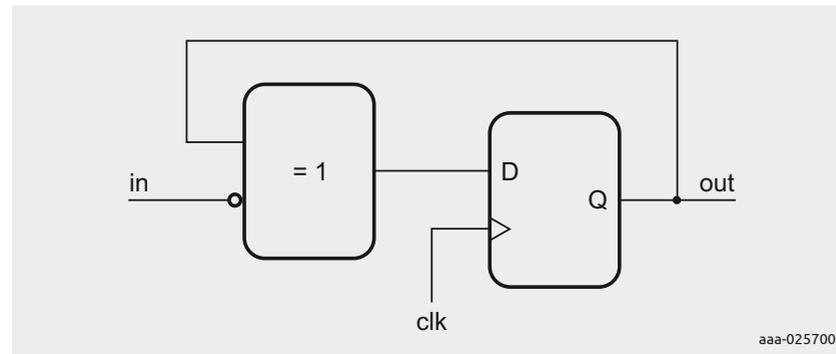
Figure 67 | NRZI(S) encoder circuit

In Table 8 an exemplary bit stream is encoded by the NRZI coder. The second row of the Table is the inverted input bit stream. The third row shows the output of the XOR. In the fourth row the coded output signal is depicted. The output bit stream shows the desired logic of a polarity toggle, which is created by a logical 0 in the input stream — with no change in the output stage for a logical 1 in the input data stream.

Table 8: Example for the NRZI(S) encoding

input	1	0	0	0	1	1	1	0	1	0	1	1	0
inverted input	0	1	1	1	0	0	0	1	0	1	0	0	1
output XOR	0	1	0	1	1	1	1	0	0	1	1	1	0
Encoder output	0	0	1	0	1	1	1	1	0	0	1	1	1

Figure 68 shows a simplified schematic of a decoder for an NRZI data stream, which detects a signal change with an output as logical state 0 and no signal change as logical state 1.

The function is realized by an XOR gate, where the data stream is connected to one input and the second input is connected to the output of a flip flop which provides the prior state of the encoder. Finally, the output of the XOR is inverted to derive the correct polarity.

Table 9 shows how the decoder works, showing the bit stream at the input in the first row, the output of the flip-flop, the output of the XOR gate before the inversion and the final output of the decoder in the last row. It is shown that the output stream of the decoding stage is identical with the input stream of Table 8.

Please note that in signal transmission it is preferable to have a DC-free system. Consequently, it is not required to have a direct galvanic connection for cable transmission between transmitter and receiver. The frequency band of the data channel does not need to start at 0 Hz but can be designed to a higher value. This ensures that data transmission can operate within a smaller frequency band.

Whenever a 0-state is transmitted, NRZI coding ensures that changes are incurred on the data during transmission. If a constant high occurs the signal can get stuck, with no oscillations occurring. For this reason, a signal change has to be forced after 6 bits in high state, which is applicable to all USB standards. Note also that seven subsequent high states indicate a bit sequence error.

aaa-025701
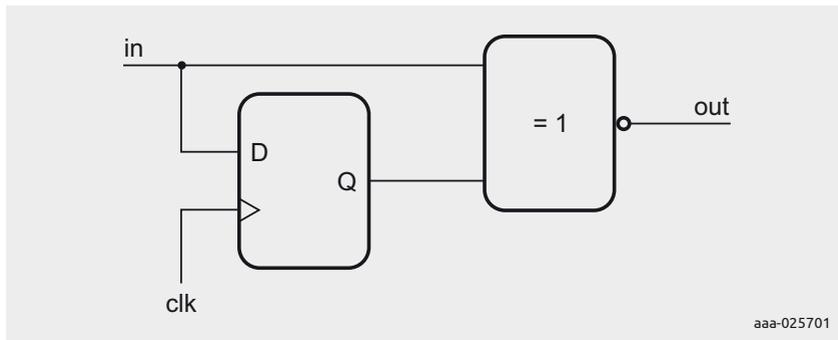
Figure 68 | Decoder schematics

Table 9: Example for NRZ decoding

input to decoder	0	0	1	0	1	1	1	1	0	0	1	1	1
output of flip-flop	x	0	0	1	0	1	1	1	1	0	0	1	1
output XOR	x	0	1	1	1	0	0	0	1	0	1	0	0
output decoder	x	1	0	0	0	1	1	1	0	1	0	1	1

Whenever D+ signal is in low state and D− is in high state, the USB bus data line state is called K-state. J-state describes the opposite condition, at which D+ is in high state and D− at in low state. Whenever both signal lines are pulled low, the system is in single-ended zero condition, referred to as SE0.

aaa-025702
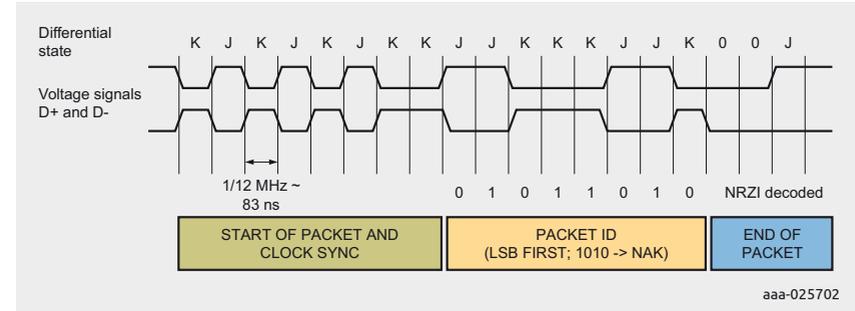
Figure 69 | Example data stream on USB 1.1 full-speed interface

Figure 69 shows a brief data stream example that transmits a NAK (Not AcKnowledged) packet at a bit rate of 12 Mbit/s, via USB 1.1 full-speed. NAK indicates that data cannot be read out (e.g. because of problems with the receiving and/or sending device/s).

Whenever real data content is transmitted, data packets are placed between the packet ID and the end-of-packet (EOP) block. The last placement of the sequence is implemented with two SE0 states, which is then followed by one idle J-state. Data transmission begins with an idle J-state: With a *00000001* sequence, i.e. with a *KJKJKJKK* sequence.

In USB 2.0 high-speed mode, the start sequence is 32 bits long, which provides more transitions. Thus, enabling the clock recovery phase-locked loop (PLL) circuit to synchronize in exact correspondence to the timing of the bit stream.

When no device is connected, the host pulls low both signal lines to ground via a 15 kΩ pull-down resistor. If a USB device is connected, one of the signal lines is pulled high via a 1.5 kΩ resistor and overwrites the pull-down state of the host.

USB 1.x speed is determined whenever D+ or D− line is pulled high via the 1.5 kΩ USB pull-up resistor. J-state signifies the idle state for USB full-speed mode; K-state signifies low-speed. A reset to SE0 condition occurs when both signal lines are pulled low by the host for 10 to 20 ms. If a USB 2.0 ready device is connected, the above described procedure for USB 1.1 devices is performed initially, but then continued with another process.

After reset, the device puts a k-state on the bus telling the host that it can handle the higher speed. After this the host toggles 3 times between J and K state to tell the USB device that the host can also support the high-speed data rate. This handshaking procedure for the speed capability of host and device is known as 'chirping' in USB literature.

8.1.2 USB 2.0 eye diagrams

The USB standard specification defines four measurement planes that are used to test a USB interface, as depicted in Figure 70. TP1 connects directly to the signal lines of the transceiver of the hub circuit board. TP2 connects the USB cable. TP3 is located directly at the input connection point of the USB device. TP4 connects directly to the pins of the receiving block of the device circuit board.

In an eye diagram measurement, an oscilloscope shows the bit transitions of a data path as an overlay of many single traces with random data content. The oscilloscope is triggered with a recovered bit clock signal because no separate clock signal is provided on an extra signal line. A data clock recovery PLL provides the data sampling clock, synchronized to data transitions.

aaa-025729
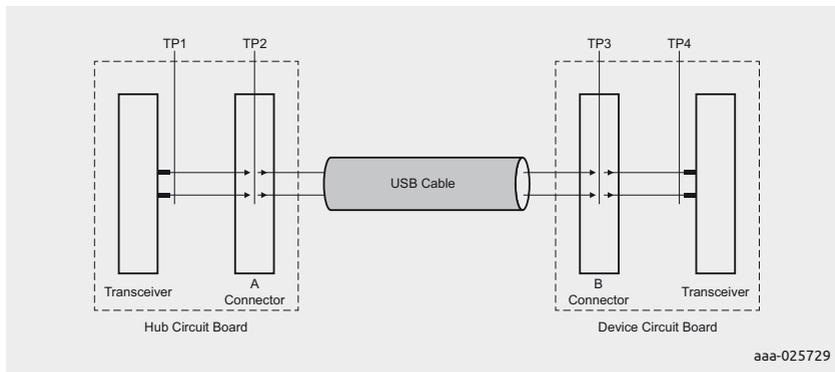
Figure 70 | Fig 11. Measurement planes for eye diagrams

The data eye diagram is a methodology that helps to analyze the signal quality of a high speed digital signal. Ideally, an eye diagram with a binary signal shows a row of rectangular boxes. However, in real scenarios the rise and fall times are not zero but are extended both by parasitic capacitances in the data path and by the limited speed of the transmitter stages.

Reflections, overlay of noise and jitter of the PLL clock, render a graph with a smaller open temporal window, the part of the eye diagram where no signal transitions occur. Data transitions are not located at exactly n times the symbol length. Jitter can have both a random distribution and a deterministic distribution, depending on its root cause. The nature of the jitter can be analyzed with a histogram. The width of the complete histogram represents the peak-to-peak jitter.

Figure 71 shows how the waveforms of transmitted data for a hub, measured at TP2, or for a device, measured at TP3, should look like. In a standard-compliant scenario, no signal traces are noticeable within the inner mask of the diagram, which is defined by points 1 to 6, as listed in Table 10. Each of these points is defined by a certain voltage and time within the unit interval. The unit interval is equal to the symbol length.

USB high speed shows:

$$\text{Tsymbol} = 1/\text{fsymbol} = 1/480\,\text{Mhz} = 2.0833\,\text{ns}$$

The temporal location is listed as a percentage value of the unit interval in the table. The nominal voltage swing of USB 2.0 is 400 mV to −400 mV. The diagram shows a second mask, which limits the signal in terms of higher voltages. The maximum voltage for the signal is ±475 mV, for a time at which no transitions occur. The voltage limit at transitions is ±525 mV, which allows some room for over- and under-shoots.

aaa-025730
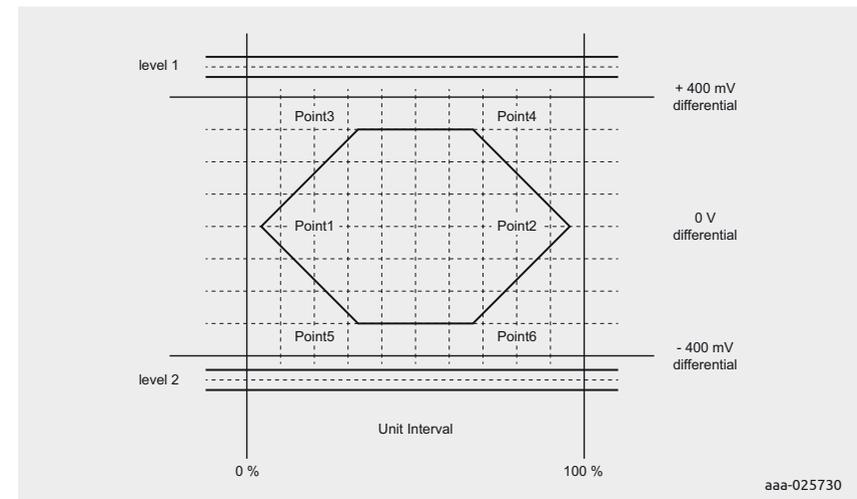
Figure 71 | Transmit waveform requirement for a hub (TP2) or a device (TP3) without a captive cable

Table 10: Parameters for the USB 2.0 transmitter eye for the test case according to Figure 69

	Voltage level (D+, D−)	Time (% of Unit Interval) 1/480 MHz = 2.0833 ns nominal
Level 1	525 mV in UI following a transition, 475 mV in all others	−
Level 2	−525 mV in UI following a transition, −475 mV in all others	−
Point 1	0V	5%
Point 2	0V	95%
Point 3	300 mV	35%
Point 4	300 mV	65%
Point 5	−300 mV	35%
Point 6	−300 mV	65%

Figure 72 shows a receiver waveform requirement scheme for a signal applied to TP4/device transceiver or to TP1/hub transceiver. The receiver mask is typically smaller than the transmitter mask, as stated above. The height of the eye is 300 mV, with a −150 mV to +150 mV range. The width of the eye is reduced to 60% of the unit interval.

Table 11 contains the details for the keep-out area for this particular test condition, which shows the smaller inner mask, as well as the upper and lower boundaries as outside limitation for the D+ and D− signal waveforms.
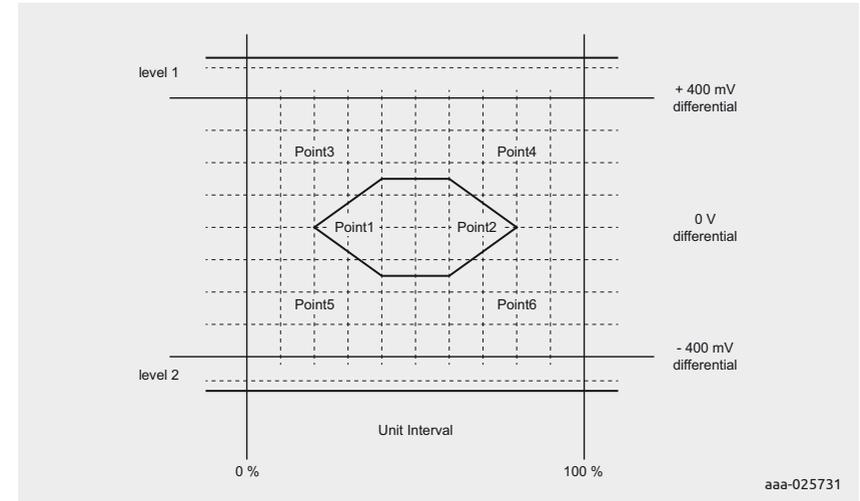
Figure 72 | Receiver waveform requirements for USB 2.0 with a signal applied at TP4 for a device transceiver or a hub transceiver with a signal applied at TP1

Table 11: Parameters for the USB 2.0 receiver eye

	Voltage level (D+, D−)	Time (% of Unit Interval) 1/480 MHz = 2.0833 ns nominal
Level 1	575 mV	−
Level 2	−575 mV	−
Point 1	0V	20%
Point 2	0V	80%
Point 3	150 mV	40%
Point 4	150 mV	60%
Point 5	−150 mV	40%
Point 6	−150 mV	60%

8.1.3 USB 3.0 and USB 3.1 interfaces

USB 3.0 and USB 3.1 use a different DC content removal method on signal lines, which is referred to as 8b10b-coding: 8-bit data is replaced by 10-bit data. Thus, redundancy is added to obtain both a DC-free bit stream and a limited disparity of transmitted 0-states and 1-states. In a row of 20 bits, the counts of the two possible states shall never differ by more than ±2.

Please note that after several 8b10b code words, the signal is completely DC-free. Thus, the number of ones and zeros is identical. The 8-bit original data is split into 5 bits, which are coded in 6 bits with a 5b6b-code. The remaining 3 bits are coded in 4 bits with a 3b4b-code. Thus, forming the final 8b10b-coding scheme.

The coding operates on a running disparity (RD): After each symbol, the count of ones and zeros differs either by 1 or −1. Table 4 lists the RD coding rules. For clarification, two processes based on the rules in Table 12, are explained:

- If a code word has a disparity of zero, no disparity change occurs for the next coded word.
- If a code word has a disparity option +/− 2, a disparity is selected that prompts a sign change for the next word. To achieve this, there must be two coding options for words, which do not have an equal number of zeros and ones.

Table 12: Rules for Running Disparity coding

Previous RD	Disparity of Code word	Disparity chosen	Next RD
−1	0	0	−1
−1	+/− 2	+2	+1
+1	0	0	+1
+1	+/− 2	−2	−1

Table 13: 5b6b code table

Input	EDCBA	RD = −1	abcdei	RD = +1
D.00	00000	100111		011000
D.01	00001	011101		100010
D.02	00010	101101		010010
D.03	00011		110001	
D.04	00100	110101		001010
D.05	00101		101001	
D.06	00110		011001	
D.07	00111	111000		000111
D.08	01000	111001		000110
D.09	01001		100101	
D.10	01010		010101	
D.11	01011		110100	
D.12	01100		001101	
D.13	01101		101100	
D.14	01110		011100	
D.15	01111	010111		101000
D.16	10000	011011		100100
D.17	10001		100011	
D.18	10010		010011	
D.19	10011		110010	
D.20	10100		001011	
D.21	10101		101010	
D.22	10110		011010	
D.23	10111	111010		000101
D.24	11000	110011		001100

Input	EDCBA	RD = −1	abcdei	RD = +1
D.25	11001		100110	
D.26	11010		010110	
D.27	11011	101110		001001
D.28	11100		001110	
D.29	11101	101110		001110
D.30	11110	011110		100001
D.31	11111	101011		010100

Table 13 above shows how the original 5-bit code words are coded into 6-bit code words. Each new 6-bit code word contains either:

• 3 zeros and ones
• 2 ones and 4 zeros
• 4 zeros and 2 ones

The 6-bit code word in column RD = +1 can be created easily by inverting all bits of the code word in column RD = −1.

Table 14: 3b4b-code table

Input	HGF	RD = −1	fghj	RD = +1
D.x.0	000	1011		0100
D.x.1	001		1001	
Dx.2	010		0101	
D.x.3	011	1100		0011
D.x.4	100	1101		0010
D.x.5	101		1010	
D.x.6	110		0110	
D.x.P7	111	1110		0001
D.x.A7	111	0111		1000

Table 14 is the coding scheme from 3-bit to 4-bit.

Please note that Table 13 and Table 14 each contain one exception to the rule. The word codes *111000* (RD = −1) and respectively *000111* (RD = +1) in Table 13 (*EDCBA* column value *00111*) each contain the same number of zeros and ones. The same applies for the word codes *0011* and *1100* in Table 14 (*HGF* column value *011*).

High-speed interfaces like PCI Express, Serial ATA, Display Port, Fibre Channel Gigabit, Ethernet and DVB make use of 8b10b-coding, which also supports AC-coupling. This makes clock recovery much easier. Clock recovery with a PLL clock generator is required in all scenarios in which no separate clock signal is sent with the data. The PLL of the data receiver needs to synchronize to the data signal transitions to allow safe sampling of incoming data.

USB high-speed, and the slower modes, make use of one differential pair with signal lines D+ and D− for data transmission, which allows half duplex data transmission. USB 3.x makes use of two differential pairs. This allows data flow in both directions in full duplex mode.

Figure 73 shows the termination of the D+ and D− lines. On both sides of the connection a 45 Ω single-ended termination to ground is implemented. This results in a 90 Ω differential termination of the signal lines. In practice, the 45 Ω serial resistor behind the LS/HS drivers are switched to ground. By doing so, the serial resistor functions as 45 Ω termination for this high-speed use case.

aaa-025703
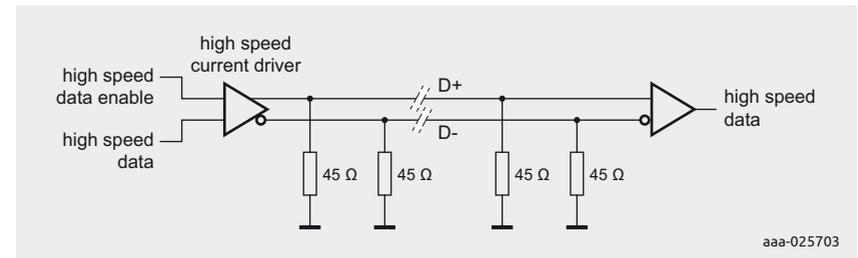
Figure 73 | Basic termination scheme for USB HS-Mode

The high-speed drivers are implemented as switched current sources that deliver 17.78 mA in single-ended high state. Figure 74 shows this basic driver structure. The high state voltage at the 45 Ω resistors in parallel operation is:

$$V_{SEhigh} = \frac{17.78\ mA}{22.5\ \Omega} = 400\ mV$$

The nominal differential voltage swing on the D+/D− signal pair is therefore ±400 mV.
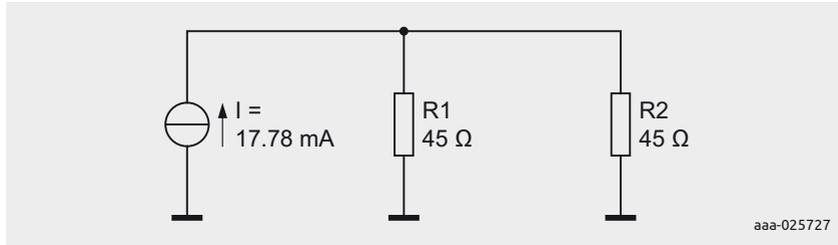
Figure 74 | HS 17.78 mA current source attached to each signal line (D+/D−)

In Figure 75 the coupling of the two differential signal pairs for the super speed signals RX and TX is depicted. At every transmitter side, the TX lines contain capacitors that realize AC-coupling for both differential connection lanes. The nominal capacitance of these capacitors is 100 nF. The figure shows the cable connection of a host and a USB device that is plugged into mated connectors.

Currently, it is practice to place additional 330 nF capacitors at the data inputs RXp and RXn and a 250 kΩ termination to ground at the cable side of the capacitors as an extension of the USB 3 standard.
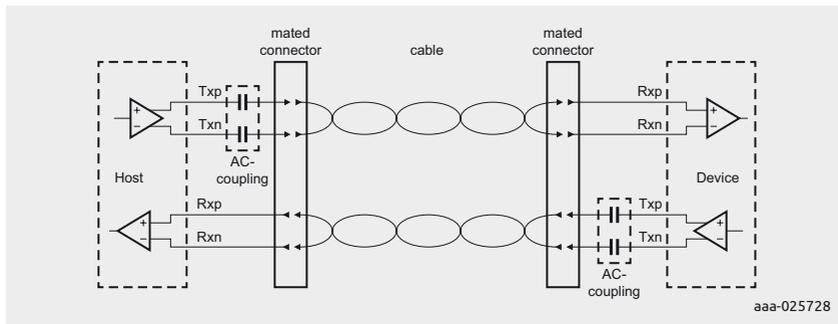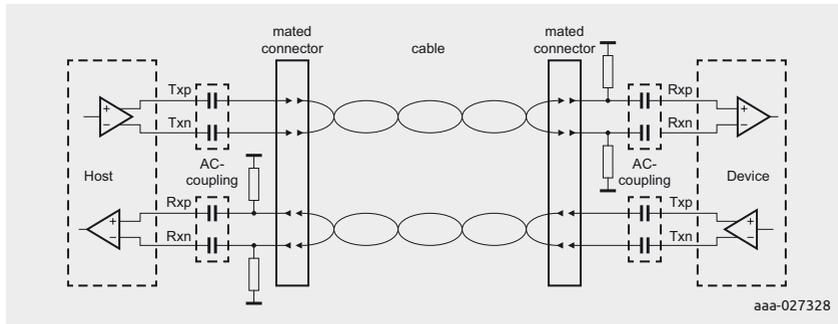
Figure 75 | Rx and Tx connection scheme for USB 3

8.1.4 USB 3.0 eye diagrams

If a connection is set up via a USB 3 Gen 1 or USB Gen 2 connection, a link training is performed as sequence, with the following steps:

1. Configuring and initializing of link
2. Bit-lock and symbol lock
3. Rx equalization training
4. Lane polarity inversion
5. Block alignment (USB Gen 2 only)

Training sequences are always 8b10b coded and not scrambled. Table 15 shows the most important normative requirements for USB 3 Gen 1 and Gen 2 transmitters.

Table 15: Basic requirements for the USB 3 transmitter

Symbol	Explanation	Gen 1, 5 Gbit/s	Gen 2, 10 Gbit/s
UI	Unit Interval	199.94ps (min) 200ps (nom) 200.06 ps (max)	99.97 ps (min) 100 ps (nom) 100.03 ps (max)
$V_{TX\text{-}Diff\text{-}PP}$	Differential peak to peak TX voltage swing	0.8V (min) 1V (nom) 1.2V (max)	0.8V (min) 1V (nom) 1.2V (max)
$V_{TX\text{-}DE\_RATIO}$	TX de-emphasis	3dB (min) 4dB (max)	3-tap FIR equalizer
$R_{TX\text{-}DIFF\text{-}DC}$	DC differential impedance	72 Ω (min) 90 Ω (nom) 120 Ω (max)	72 Ω (min) 90 Ω (nom) 120 Ω (max)
$C_{AC\text{-}COUPLING}$	AC coupling capacitor	75nF−200nF	75nF−265nF
$T_{TX\text{-}EYE}$	Transmitter eye width	0.625 UI (incl. all jitter sources)	0.625 UI (incl. all jitter sources)

Table 16 is the equivalent list for the receiver side of the super-speed USB interface. The minimum height of the receiver eye is quite low. The open width is also much smaller compared to USB super-speed.

Table 16: Basic requirements for the USB 3 receiver

Symbol	Explanation	Gen 1, 5 Gbit/s	Gen 2, 10 Gbit/s
UI	Unit Interval	199.94ps (min) 200ps (nom) 200.06 (max)	99.97ps (min) 100ps (nom) 100.03ps (max)
$V_{RX-DIFF-PP-POST-EQ}$	Differential peak to peak RX voltage swing	100mV (min)	70mV (min)
RX equalizer	receiver equalizer	0dB−6dB	0dB−6dB
T_j	total jitter	0.66 unit intervals	0.714 unit intervals
$R_{RX-DIFF-DC}$	DC differential impedance	72 Ω (min) 90 Ω (nom) 120 Ω (max)	72 Ω (min) 90 Ω (nom) 120 Ω (max)
$C_{AC-COUPLING}$	AC coupling capacitor	75nF−200nF	75nF−265nF

Figure 76 shows the receiver mask for 5 Gbit/s, and Figure 77 depicts the related mask for 10 Gbit/s. The mask in the USB 3 Gen 1 scenario has a minimum eye height of 100 mV whereas the eye height in USB 3 Gen 2 scenario is only 70 mV. The minimum eye width is 0.34 unit intervals, respectively 0.286 unit intervals, in the 10 Gbit/s scenario. Moreover, the shape of the mask is also different. In the 5 Gbit/s scenario the mask has the shape of a rhombus whereas the shape in the 10 Gbit/s scenario is like the USB 2.0 scenario, with a 0.1-unit interval width for the upper and lower mask borders.
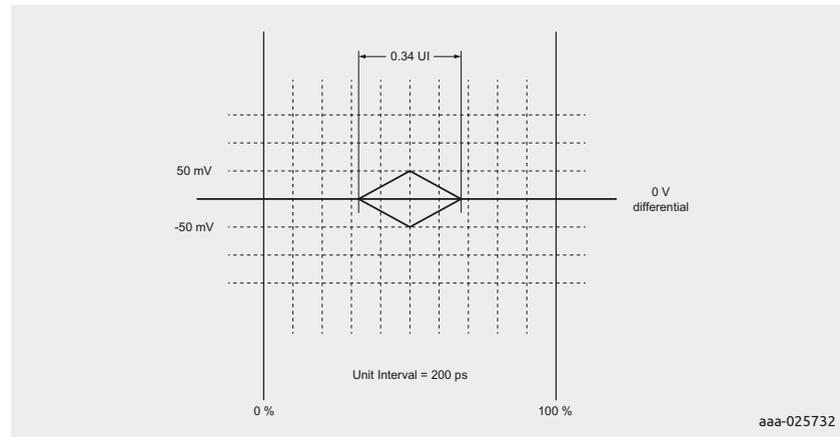
Figure 76 | Mask diagram of USB 3 Gen 1 scenario; 5 Gbit/s
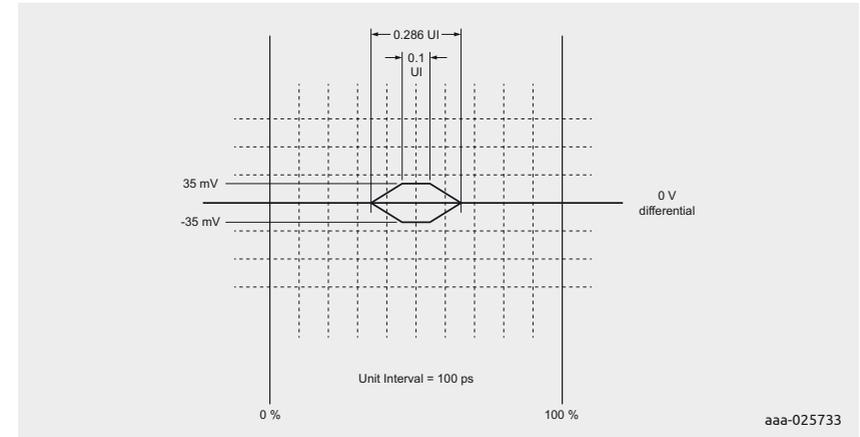
Figure 77 | Mask diagram of USB 3 Gen 2 scenario; 10 Gbit/s

8.1.5 USB Type-C

The user-friendly 24-pin connector allows reversible plugs. The innovative connector type supports up to USB 3 Gen 2 speed at 10 Gbit/s, as well as USB 2.0 power delivery. For a further data speed increase of a factor 2, USB 3.2 introduces 2 lanes for RX and TX running in parallel. Full-feature cables are electronically marked with an identification IC. Alternate modes can be set up via the dedicated configuration channels, with vendor defined messages (VDMs).

The Type-C connector can support various other standards beside USB. They are Display Port, Thunderbolt 3, MHL, PCI Express and Base-T Ethernet. Various dongles that convert from USB Type-C to legacy connectors or other interface standards like HDMI are available on the market.

In Table 17 the pin assignment of USB Type-C connector is listed. Figure 78 shows a front view of a Type-C plug. The 24 pins are organized in two groups of 12 pins each, i.e. group A and group B. Pins are available for four differential pairs with Super Speed operation (two lanes each for RX_P/RX_N and TX_P/TX_n). Moreover, two pins for USB 2.0 lane pair (Dp/Dn), two configuration channel pins (CC1 and CC2) and two sideband usage (SBU) pins. Additionally, 4 Ground and 4 V_{BUS} pins that ensure low resistance for the power path.

Table 17: USB Type-C pin assignment

Pin number	Signal name	Explanation
A1	GND	Ground
A2	SSTXp1	Super Speed differential TX pair 1, positive signal
A3	SSTXn1	Super Speed differential TX pair 1, negative signal
A4	V_{BUS}	Bus Power line
A5	CC1	Configuration Channel 1
A6	Dp1	USB 2.0 differential pair 1, positive signal
A7	Dn1	USB 2.0 differential pair 1, negative signal
A8	SBU1	Sideband Usage signal 1
A9	V_{BUS}	Bus Power line
A10	SSRXn2	Super Speed differential RX pair 2, negative signal
A11	SSRXp2	Super Speed differential RX pair 2, positive signal
A12	GND	Ground
B1	GND	Ground
B2	SSTXp2	Super Speed differential TX pair 2, positive signal
B3	SSTXn2	Super Speed differential TX pair 2, negative signal
B4	V_{BUS}	Bus Power line
B5	CC2	Configuration Channel 2
B6	Dp2	USB 2 differential pair 2, positive signal
B7	Dn2	USB 2 differential pair 2, negative signal
B8	SBU2	Sideband Usage signal 2
B9	V_{BUS}	Bus Power line
B10	SSRXn1	Super Speed differential RX pair 1, negative signal
B11	SSRXp1	Super Speed differential RX pair 1, positive signal
B12	GND	Ground

Figure 78 | Pinout and front view of USB Type-C connector

As soon as the connection is established, the orientation of the cable connection is detected via the CC pins. The Type-C cable has one physical CC wire only. With this single connection both ends of the cable can detect the appropriate super-speed lines needed for data exchange:

For example, the connection process of a downstream facing port (DFP) to an upstream facing port (UFP) occurs, as follows:

1. DFP to UFP attach/detach detection
2. Plus orientation/cable twist detection
3. Initial DFP-to-UFP (host to device) and power relationship detection
4. USB Type-C VBUS current detection and usage
5. USB power delivery (PD) communication
6. Discovery and configuration of functional extensions

Figure 79 depicts a DFP to UFP connection scenario. On the DFP side, pull-up resistors Rp are implemented towards a positive supply voltage. On the other end of the cable pull-down resistors are connected to ground.

Please note that as default, a current source can be configured instead of using RP pull-up resistors. The node with the higher voltage of the two

CC pins indicates the direction of the connection. Ra is available for powered cables and audio adapters, as shown in Table 20 below. The Rp value can detect 5 V-current capability.
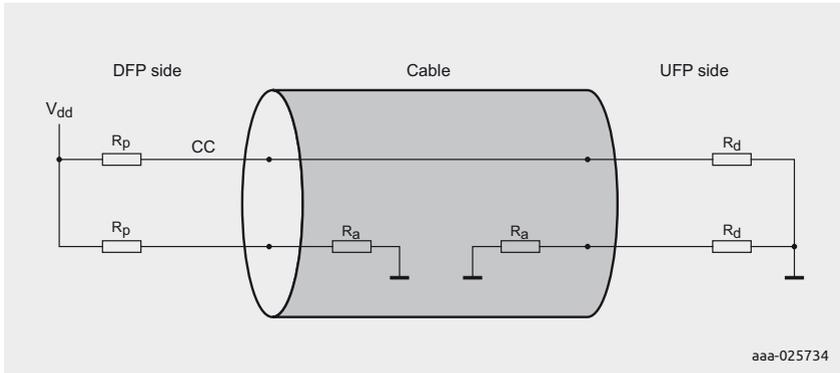
Figure 79 | DFP-UFP CC model connection

In Table 18 the value for the pull-up resistor Rp and the related power rating is shown for either a 5 V or 3.3 V supply connected to the pull-up as supply voltage. Alternatively, the standard also allows the use of a current source instead of pull-up resistors.

Table 19 defines how the pull-down resistor Rd is specified. The nominal termination is a 5 kΩ resistor. Voltage clamping does not allow detection of power capability. For this function the tolerance of Rd needs to be ±10% at least.

Table 18: Down-stream port (DFP) Rp requirements

DFP Dedication	Current Source to 1.7 V – 5.5 V	Pull-up resistor to 4.75 V – 5.5 V	Pull-up resistor to 3.135 V – 3.465 V
Default USB power	80 µA +/− 20%	56 k +/− 20%	36 +/− 20%
1.5 A/5 V	180 µA +/− 8%	22 k +/− 5%	12 +/− 5%
3.0 A/5 V	330 µA +/− 8%	10 k +/− 5%	4.7k +/− 5%

Table 19: Up-stream port (UFP) Rd requirements

Rd implementation	Nominal value	Power detection capability	maximum voltage at the CC pin
+/− 20% voltage clamp	1.1 V	no	1.32 V
+/− 20% resistor to GND	5.1 kΩ	no	2.18 V
+/− 10% resistor to GND	5.1 kΩ	yes	2.04 V

The Ra termination resistor has a nominal resistance of 1 kΩ, as shown in Figure 79. It is often applied via a JFET that limits the current after detection process, as shown in Figure 80.

As soon as the pitch-off voltage of the depletion FET is reached, the current increases the voltage level in Ra at the source of the depletion FET until it clamps the current to a maximum value. Thus, power loss is reduced whenever the 5 V supply voltage Vconn is switched to the CC line.
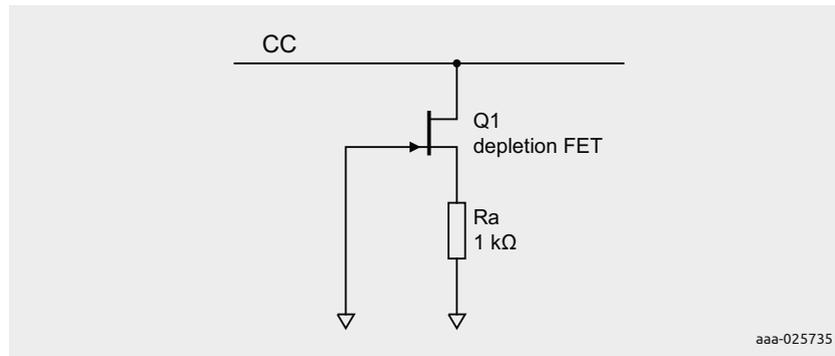
Figure 80 | Ra termination solution

Table 20 is a list of states that result from CC line termination in a DFP-UFP connection.

Table 20: CC connection model for a DFP-UFP scenario

CC1	CC2	State
open	open	Nothing attached
Rd	open	UFP attached
open	Rd	UFP attached
Ra	open	Powered cable, no UFP attached
open	Ra	Powered cable, no UFP attached
Ra	Rd	Powered cable and UFP attached
Rd	Ra	Powered cable and UFP attached
Rd	Rd	Debug accessory Mode attached
Ra	Ra	Audio adapter accessory Mode attached

8.2 HDMI interfaces

8.2.1 Introduction to HDMI interfaces

HDMI is a digital interface in consumer and computing applications. It is similar to DVI but also includes consumer electronics control (CEC). Video data is transmitted without data compression whereas audio can be used with or without data compression.

The interface is HDCP copy-protected. High-speed data is transmitted via transition minimized differential signaling (TMDS) lines. The interface uses three TMDS lanes and one additional channel for the clock signal.

As of HDMI 1.4, HDMI also supports an ethernet data channel on the HEC lane. The display data channel (DDC), that is similar to I2C, is used to exchange information. The resolution compatibility is supported whenever an HDMI connection is established. Thus, extended display identification data (EDID) can be read out.

8.2.2 Contact assignment for connectors

In Table 21 the contact assignments for Type A connectors, which are the most commonly used connectors in TVs, monitors, DVD players and computers, are listed. Figure 81 shows an HDMI connector front view. Type D micro-HDMI connectors are used for tablets, cameras and other mobile devices.

Table 21: Contact assignment for HDMI Type A and Type C connector

Contact Type A	Contact Type D	Signal description
Pin 1	Pin 3	TMDS Data2+
Pin 2	Pin 4	TMDS Data2 shielding
Pin 3	Pin 5	TMDS Data2−
Pin 4	Pin 6	TMDS Data1+
Pin 5	Pin 7	TMDS Data1 shielding
Pin 6	Pin 8	TMDS Data1−
Pin 7	Pin 9	TMDS Data0+
Pin 8	Pin 10	TMDS Data0 shielding

Contact Type A	Contact Type D	Signal description
Pin 9	Pin 11	TMDS Data0−
Pin 10	Pin 12	TMDS clock+
Pin 11	Pin 13	TMDS clock shielding
Pin 12	Pin 14	TMDS clock−
Pin 13	Pin 15	CEC
Pin 14	Pin 2	reserved (HDMI1.0–1.3), HEC data− (HDMI 1.4)
Pin 15	Pin 17	DDC clock (I²C-Bus, SCL)
Pin 16	Pin 18	DDC data (I²C-Bus, SDA)
Pin 17	Pin 16	Ground for DDC, CEC and HEC
Pin 18	Pin 19	−5 V supply with 55 mA maximum current
Pin 19	Pin 1	Hot-Plug-Detection (all standards), HEC Data+ (HDMI 1.4)

Figure 81 | Pinout and front view of HDMI connector

8.2.3 HDMI key parameters connection structure

HDMI introduced consecutively additional standards with higher data rates that are necessary for high resolution displays. Table 22 shows a brief overview of HDMI versions and contains maximum pixel rates, as well as maximum clock rates and TMDS bit rates. The Table also lists maximum screen resolutions for consumer applications and supported maximum color depths of the pixels. TMDS lines have a ratio between clock and bit rate of factor 10 for HDMI 1.4, and factor 14 for HDMI 2.0.

Table 22: List of HDMI key parameters for the different versions

HDMI version	1.0	1.1	1.2	1.3	1.4	2.0	2.1
Maximum pixel clock rate (MHz)	165	165	165	340	340	600	no extra clock channel
Maximum TMDS bit rate per lane including 8b/10b coding overhead (Gbit/s)	1.65	1.65	1.65	3.4	3.4	6	12
Maximum total TMDS throughput including 8B/10b coding overhead (Gbit/s)	4.95	4.95	4.95	10.2	10.2	18	48
Maximum audio throughput bit rate (Mbit/s)	36.86	36.86	36.86	36.86	36.86	49.152	49.152
Maximum video resolution over 24 bit/pixel single link	1920* 1200 p/ 60 Hz	1920* 1200 p/ 60 Hz	1920* 1200 p/ 60Hz	2560* 1600 p/ 60 Hz	4096* 2160 p/ 30 Hz	4096* 2160 p/ 60 Hz	7680* 4320 p/ 60 Hz
Maximum color depth (bit/pixel)	24	24	24	48	48	48	48

Figure 82 shows the basic HDMI TMDS data connection structure of transmitters and sink connectors. The transmitter has a switched current source of 10 mA. A differential signal connection with matched impedance builds the data path to the receiver. The receiver terminates each signal line of the differential interface with 50 Ω to a 3.3 V supply line.

This leads to a single-ended nominal voltage swing of:

$$V_{SE} = 10 \text{ mA} \cdot 50 \text{ } \Omega = 500 \text{ mV}$$

Consequently, the nominal differential voltage swing is 1 V, which is twice the value of a single-ended data line. The differential nominal termination is 100 Ω, which is twice the value of the single-ended pull-up resistors of the HDMI sink connectors. The impedance matching must be kept in an 85 Ω to 115 Ω window, i.e. 100 Ω ±15%; to comply with HDMI specification.


aaa-025736
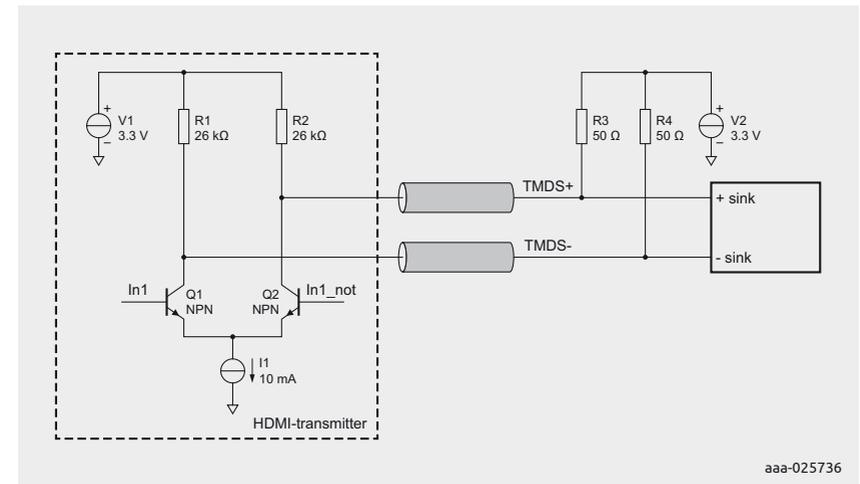
Figure 82 | HDMI transmitter to receiver driver structure

Figure 83 shows the HDMI 1.4 transmitter mask, as well as upper and lower limits of the TMDS line voltage. The eye has a minimum height of 400 mV, and a width of 0.7 unit intervals.
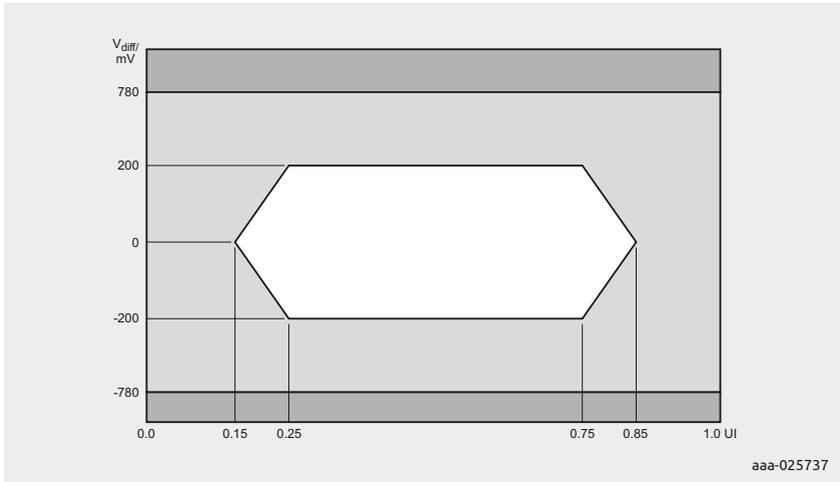
Figure 83 | HDMI 1.4 transmitter eye diagram mask

Figure 84 depicts the HDMI 1.4 receiver mask. Eye height is 300 mV (±50 mV) and eye width has to be at minimum 50% of the unit interval.
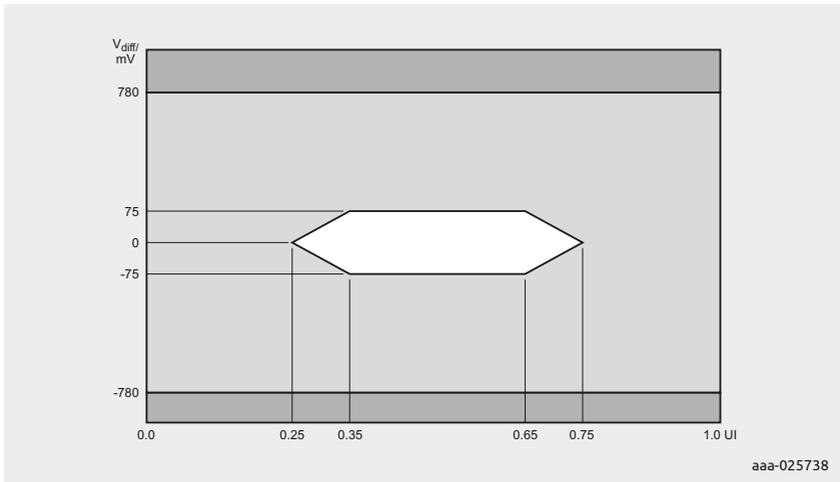
Figure 84 | HDMI 1.4 receiver eye diagram mask

Figure 85 shows the set-up of eye diagrams for eye diagram measurements with HDMI 2.0 at the source test points. TP1 is located on the receptacle plug of the pattern generator, with the test point adapter (TPA). A cable emulator based on worst-case conditions is placed between TPA-P and reference cable equalizer, followed by the TP1_EQ.
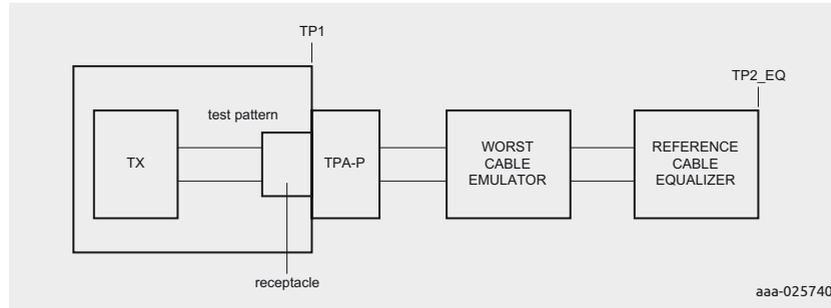
Figure 85 | HDMI Source Test point for Eye Diagram measurement

Figure 86 depicts the HDMI 2.0 mask diagram for test point TP2_EQ. Eye height H and eye width V depend on the HDMI bit rate, as shown in Table 23. To achieve the maximum bit rate of 6 Gbit/s, a minimum eye height of 150 mV and a maximum data jitter of 0.6 unit intervals are necessary; with total data jitter $T_j = 1 - H$.
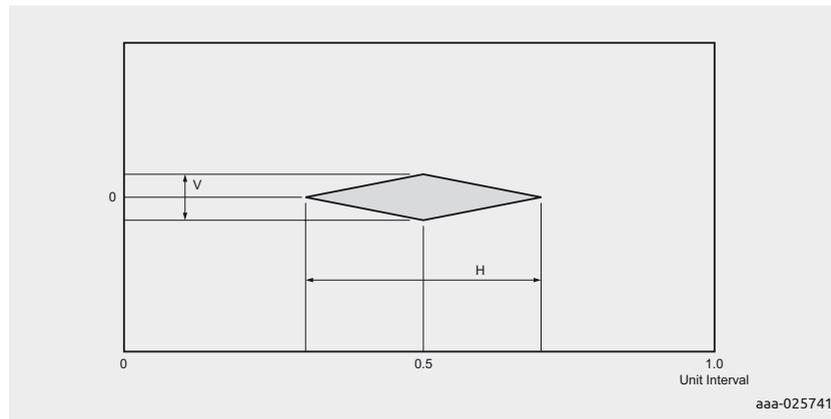
Figure 86 | HDMI2.0 mask for Eye Diagram measurements

Table 23: Mask size in dependency of the Bit Rate (Gbit/s)

TMDS Bit Rate (Gbit/s)	Mask width H (UI)	mask height V (mV)
3.4 < bit rate ≤ 3.712	0.6	335
3.712 < bit rate ≤ 5.94	−0.0332 * (bit rate)² + 0.2312 * (bit rate) + 0.1998	−19.66 * (bit rate)² + 106.74 * (bit rate) + 209.58
5.94 < bit rate ≤ 6.0	0.4	150

8.3 MIPI interface

8.3.1 Introduction to MIPI interfaces

The MIPI Alliance comprises several companies that define a data communication standard for interfacing processor and chip-sets to peripheral components such as cameras, sensors and displays. Application areas include mobile devices like smartphones, tablets and embedded systems like TVs.

Although most MIPI interfaces are not normally used for external interfaces with direct access for users, ESD protection is applied to safeguard against ESD strikes entering a device via housing gaps or in case of an opened cover. Major key facts for the physical layer of MIPI standards D-PHY, M-PHY and C-PHY are discussed in the following chapters.

8.3.2 MIPI D-PHY

MIPI D-PHY [18] is a synchronous connection between a master and slave, and the master provides the clock signal as a unidirectional signal. One or more data lanes can be used for data transmission. The minimum configuration consists of two differential signal connections or lanes, so one clock lane and at least one data lane. The direction of data flow can be unidirectional and bidirectional. Data flow direction is indicated by an exchange of token in half-duplex mode. The data speed in reverse direction is a fourth of forward direction.

A low voltage level signal is transmitted in High-Speed mode transferring data in a burst mode. A so-called Low-Power Signaling mode is foreseen for transmission of control commands. The specification does not mention a fixed maximum data rate per lane, but indicates a range from 80 to 1500 Mbit/s. If a higher data rate is required, the number of differential data pairs has to be increased.

Figure 87 shows an example for the line levels on a signal line of MIPI D-PHY. The red part of the signal shows a High-Speed data burst, whereas the blue part shows a Low-Power signaling event.
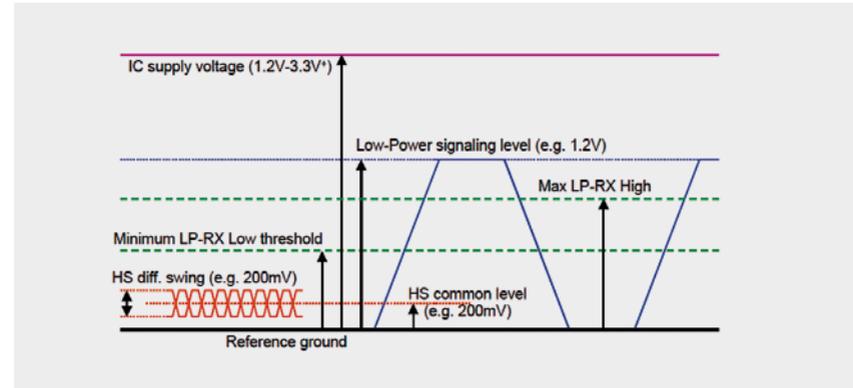
Figure 87 | Line levels for MIPI D-PHY

In Table 24 the lane states are listed. A data lane can operate in either High-Speed mode or Low-Power mode. High speed data transmission starts and stops with Stop state LP-11, which is a single ended high-state on both lines of the differential pair.

The sequence to be sent for High-Speed operation is LP-11 (stop), LP-01 (high speed request), LP-00 (bridge), and the interface stays in High-Speed mode until a stop command is received. The Control Mode is the default condition of the interface, while Escape Modes can be entered via a request sent in Control Mode.

Table 24: List of lane states for MIPI D-PHY

State Code	Line Voltage Levels		High-Speed	Low Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	not applicable	not applicable
HS-1	HS High	HS Low	Differential-1	not applicable	not applicable
LP-00	LP Low	LP Low	not applicable	Bridge	Space
LP-01	LP Low	LP High	not applicable	HS-Request	Mark-0
LP-10	LP High	LP Low	not applicable	LS-Request	Mark-1
LP-11	LP High	LP High	not applicable	Stop	not applicable

On the transmitter side, the maximum output voltage in high state VOH in Low-Power mode is 1.3 V, while the minimum level for the low state VOL is −50 mV as depicted in Table 25.

Table 25: Transmitter DC characteristics for Low-Power Mode

Parameter	Description	min	nominal	max
V_{OH}	output level high-state	1.1 V	1.2 V	1.3 V
V_{OL}	output level low-state	−50 mV	0 mV	50 mV

On the receiver side, the minimum input voltage in logical high-state VIH in Low-Power mode is 880 mV. The input level for the logical low-state has to stay below 330 mV, as Table 26 shows.

Table 26: Receiver DC characteristics for Low-Power Mode

Parameter	Description	min	nominal	max
V_{IH}	input level high-state	880 mV	–	–
V_{IL}	input level low-state	–	–	300 mV

Table 27 lists the most important transmitter DC characteristics. The differential lines have a nominal common mode voltage of 200 mV overlaid with the HS signal of 100 mV single-ended swing, which means 200 mV nominal differential swing amplitude.

Table 27: High-Speed transmitter DC characteristics

Parameter	Description	min	nominal	max
V_{CMTX}	HS transmitter static common mode voltage	150 mV	200 mV	250 mV
$|V_{DD}|$	HS transmitter differential voltage	140 mV	200 mV	270 mV
V_{OHHS}	HS output high-level voltage	–	–	360 mV
Z_{OS}	single ended output resistance	40 Ω	50 Ω	62.5 Ω
ΔZ_{OS}	single ended output resistance mismatch	–	–	10%

On the receiver side, at least +/− 70 mV are required to exceed the thresholds for the differential voltage for logical high or low state as depicted in Table 28.

Table 28: High-Speed receiver DC characteristics

Parameter	Description	min	nominal	max
V_{CMRX}	Common mode voltage HS receive mode	70 mV	–	330 mV
V_{IDTH}	Differential input high state threshold	–	–	70 mV
V_{IDTL}	Differential input low state threshold	−70 mV	–	–
V_{IHHS}	Single-ended input high voltage	–	–	460 mV
V_{ILHS}	Single-ended input low voltage	−40 mV	–	–
Z_{ID}	Differential input impedance	80 Ω	100 Ω	125 Ω

8.3.3 MIPI M-PHY

MIPI M-PHY [19] is the successor of the MIPI D-PHY standard. It addresses the growing demand for higher data rates per lane, better power efficiency and more flexibility. It uses a synchronous connection between a master and slave. The clock signal is generated via a clock PLL, so there is no dedicated clock signal transmitted from a master as with D-PHY interfaces.

Figure 88 gives an example of a MIPI M-PHY interface in which unidirectional lanes are used as data connections. Every lane connects an M-TX transmitter block to an MN-RX receiver block. For higher data rates several lanes can be foreseen in both directions.
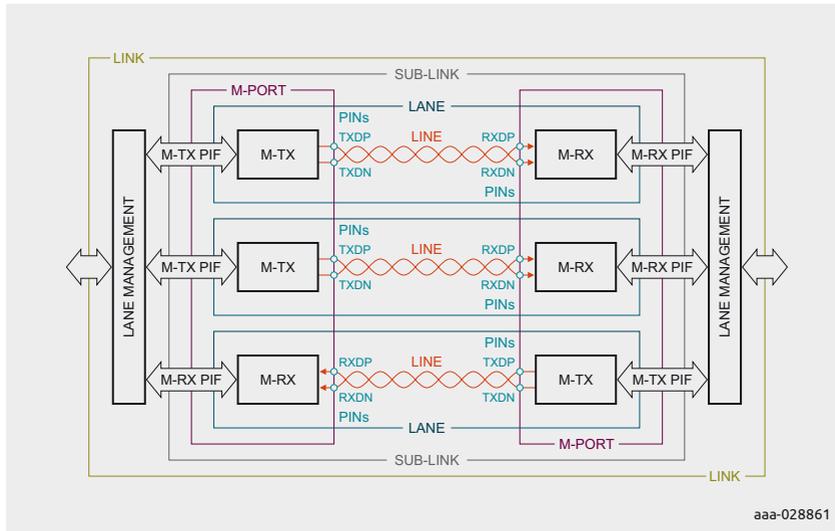
Figure 88 | MIPI M-PHY example for lane structure

Data are transmitted in the so-called HS-Burst state in HS-Mode encoded in 8b10b and put on the signals lines in a NRZ signaling. There are two series defined with related data rates that are denoted as a GEAR for each couple. The different supported data rates are listed in Table 29. shows a brief overview of HDMI versions and contains maximum pixel rates, as well as maximum clock rates and TMDS bit rates. The Table also lists maximum screen resolutions for consumer applications, and support

Table 29: High-Speed burst data rate, M-PHY series and GEARs

Rate A-series (Mbit/s)	Rate B-Series (Mbit/s)	High-Speed GEARs
1248	1457.6	HS-G1 (A/B)
2496	2915.2	HS-G2 (A/B)
4992	5830.4	HS-G3 (A/B)
9984	11680.8	HS-G4 (A/B)

Figure 89 shows the termination scheme of MIPI M-PHY. The TX drivers switch one of the differential lines to ground and the other line to V_{LD} depending on the differential lane state. Each driver output has a serial resistor R_{SE_TX} connected to the outgoing signal line. $40\,\Omega$ is the minimum value for R_{SE_TX}, the maximum allowed value is $60\,\Omega$. The receiver side RX only requires a termination in the High-Speed Mode (HS Mode).
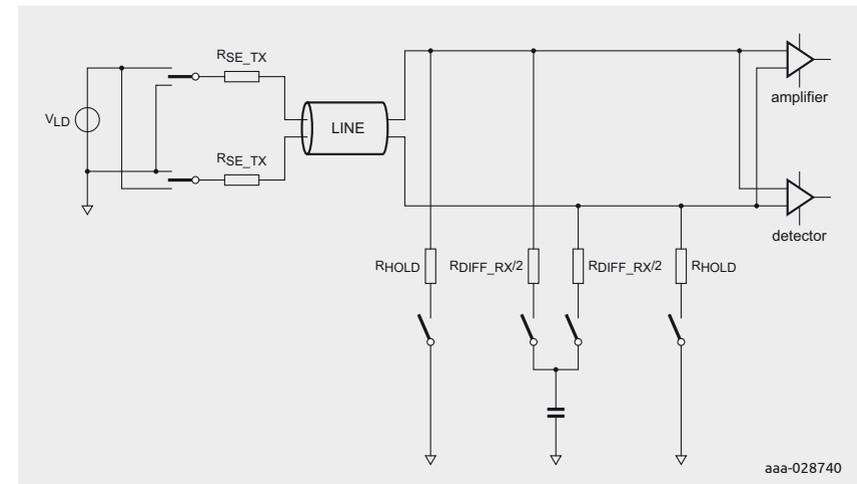
Figure 89 | MIPI M-PHY termination scheme

Figure 90 shows the transmitter side MIPI M-PHY eye diagram for the High-Speed mode in GEAR 3 and GEAR 4. The minimum eye height is 80 mV. The temporal eye width has to be 0.55 unit intervals in GEAR 3 and 0.5 unit intervals in GEAR 4. These key parameters are listed in Table 30.
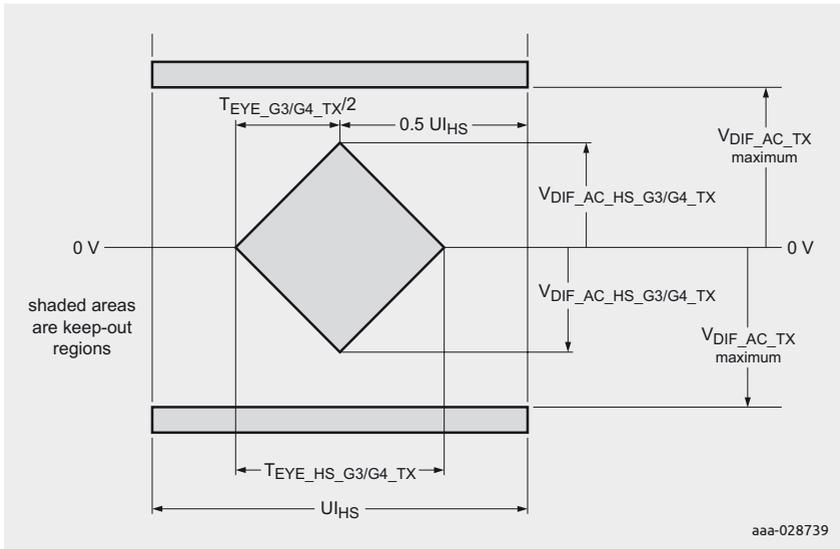

Figure 90 | M-PHY TX eye diagram for HS-Mode GEAR 3and 4

Table 30: High-Speed GEAR 3 and GEAR 4 electrical TX key parameters

Parameter	Value	Description
$V_{DIF\_AC\_HS\_G3/4\_TX}$	40 mV, minimum	Differential TX AC voltage in HS-G3/4
$V_{DIF\_AC\_HS\_G4\_TX}$	40 mV, minimum	Differential TX AC voltage in HS-G4
$T_{EYE\_HS\_G3\_TX}$	0.55 Unit intervals (UI)	Transmitter eye opening in HS-G3
$T_{EYE\_HS\_G4\_TX}$	0.5 Unit intervals (UI)	Transmitter eye opening in HS-G4

The receiver side eye diagram looks like the transmitter side diagram. For the highest data speed of MIPI M-PHY HS-Speed GEAR 4, the height of the eye is the same as the transmitter eye height. It is twice $V_{DIF\_AC\_HS}$, equal to 40 mV as minimum requirement. The open eye width $T_{EYE\_HS\_G4\_RX}$ is defined as 1 - TJ_{RX} measured in unit intervals. TJ_{RX} is lower or equal to 0.52 unit intervals for GEAR 4. This means that the open eye is 0.48 unit intervals wide in temporal direction as minimum requirement.

8.3.4 MIPI C-PHY

MIPI C-PHY [20] uses three signal lines instead of two lines for conventional differential data lanes. This allows a higher data rate without needing 4 signal lines for two parallel standard differential lanes. MIPI C-PHY achieves 2.28 bits per symbol. It has some similarities with MIPI D-PHY for the transition between low power modes and high-speed modes. Unlike the D-PHY standard, no separate clock channel is provided. The combination of signal voltages on the lines changes from symbol to symbol. This makes it comparatively simple to regenerate the clock signal because of transitions after each symbol.

The maximum symbol rate is 3 GSps (Giga symbols per second). This symbol rate is the relevant value for the frequency spectrum to be considered for the selection of ESD protection devices. 1.5 GHz is the highest frequency of the fundamental wave in high speed mode.

Table 31 shows the signal voltages for the signal lines A, B and C in the columns wire amplitude, the receiver differential input voltages A-B, B-C and C-A, and the related digital output stages in the left three columns. The line voltages are all combinations of 0.25 V, 0.5 V and 0.75 V for the three wires. The corresponding 3 voltage differences have a sum of zero for every state +x, −x, +y, −y, +z or −z. A positive difference corresponds to a digital high state for the digital output of the receiver.

Table 31: Signal voltage and differential voltages for the six C-PHY lane states

Wire State	Wire Amplitude			Receiver differential input voltage			Receiver digital output		
	A	B	C	A-B	B-C	C-A	Rx-AB	RX-BC	RX-CA
+x	3/4 V	1/4 V	1/2 V	+1/2 V	−1/4 V	−1/4 V	1	0	0
−x	1/4 V	3/4 V	1/2 V	−1/2 V	+1/4 V	+1/4 V	0	1	1
+y	1/2 V	3/4 V	1/4 V	−1/4 V	+1/2 V	−1/4 V	0	1	0
−y	1/2 V	1/4 V	3/4 V	+1/4 V	−1/2 V	+1/4 V	1	0	1
+z	1/4 V	1/2 V	3/4 V	−1/4 V	−1/4 V	+1/2 V	0	0	1
−z	3/4 V	1/2 V	1/4 V	+1/4 V	+1/4 V	−1/2 V	1	1	0

Figure 91 shows how the six lane states are realized to achieve the voltages for the signal lines according to Table 31. At the transmitter side the lines can be switched to the driver voltage V+ or ground via a 50 Ω termination via a pull-up (PU) or pull-down (PD) switching FET. Together with the receiver termination of 2 × 50 Ω between the two comparator inputs, the voltage levels +/− 1/4 V and +/− 3/4 V are generated. For example, in the line state +x, the driver voltage +V is switched to the A line via a 50 Ω resistor by the switch PU_A. The positive input of the comparator RX_AB is connected to a divider created by this 50 Ω PU and the 100 Ω between the comparator inputs plus the PD resistor of 50 Ω from the switch PD_B connected to ground. This results in the 3/4 +V level on the A signal wire. A second stage with 100 Ω PU and PD resistors and switching FETs create the 1/2 +V voltage for a signal line. This can be seen for example in state +x for the C signal wire.

If +V is connected to line A (via PU_A) and the switch to ground is active at line B (PD_B), the state +x is called A to B as well. For the opposite polarities the state −x can be nominated B to A. The corresponding receiver, RX_AB in the example discussed, the receiver difference is either +1/2 +V or −1/2 +V. This is the background for so-called positive or negative polarity like the left and right separation in Figure 91. For the second row with the two y states the same system can be applied for the wires B and C and the polarity is reflected in the polarity of the differences at the inputs of RX_BC.


aaa-028862
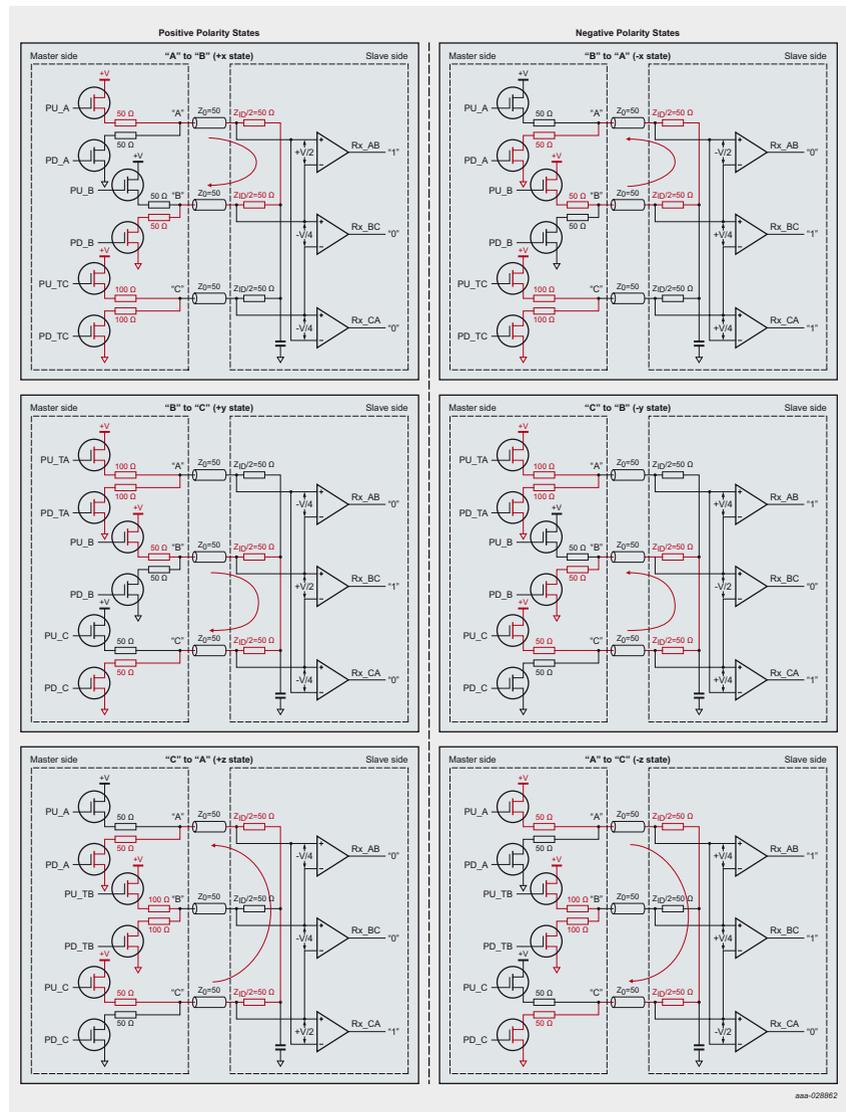
Figure 91 | The six C-PHY wire states in nominal condition, with driver and receiver side structure

From the six possible states there are five possible transitions to any other state. These transitions are depicted in Figure 92. Like in Figure 91 the states are divided in positive and negative polarities in the inner circle and the negative states outside the inner circle.
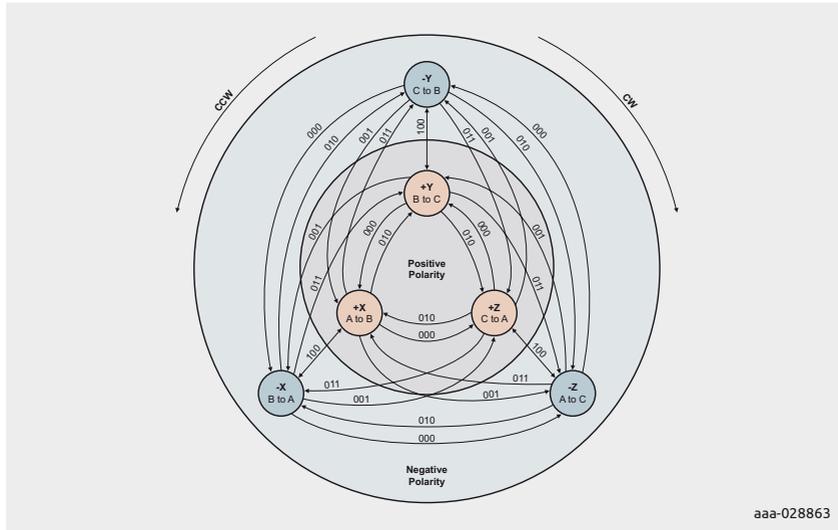

Figure 92 | All six MIPI states with all possible five transitions

Each transmitted symbol is represented by a 3-bit number for the transitions between the six wire states with the values 000, 001, 010, 011 and 100. These values can be found in blue at the transition arrows. C-PHY defines three state change parameters which are flip, rotate and polarity, represented in the three bits of the transition values.

The least significant bit indicates a polarity change, so a change from light grey area to dark grey or the opposite direction in the diagram. The next significant bit indicated the direction of rotation in the diagram for the wire state. If it is clockwise (CW in diagram) the bit is set to 1, in the counter-clock direction (CCW) it is 0. Finally, the most significant bit stands for a flip of the same state in polarity. This is, for example, a change from state +x to −x or vice versa. The flip transitions are represented with the value 100. Polarity change and rotation bits are put to zero.

Table 32 shows all five transitions with the symbol values in the left column from every wire state in time interval N-1 to any other present state. The right column indicates which facts can be assigned to each transition in terms of direction of rotation and polarity change, as well as the flip case, indicated also as same phase in the C-PHY standard.

Table 32: Transitions from previous state to present state

Symbol Input Value	Previous Wire state, interval N-1						description of transition facts
	+x	−x	+y	−y	+z	−z	
000	+z	−z	+x	−x	+y	−y	Rotate CCW, pol. is the same
001	−z	+z	−x	+x	−y	+y	Rotate CCW, pol. is opposite
010	+y	−y	+z	−z	+x	−x	Rotate CW, pol. is the same
011	−y	+y	−z	+z	−x	+x	Rotate CW, pol. is opposite
1xx	−x	+x	−y	+y	−z	+z	same phase, pol. is opposite

Figure 93 shows a receiver eye diagram for MIPI C-PHY in high speed mode. The height of the eye has to be at least 80 mV which is twice V_{IDTH} threshold voltages for the differential receivers. The eye width $T_{EYE\_WIDTH\_RX}$ is at least 0.5 unit intervals.

The maximum signal voltage on a line can be 1.35 V which is related to LP mode.
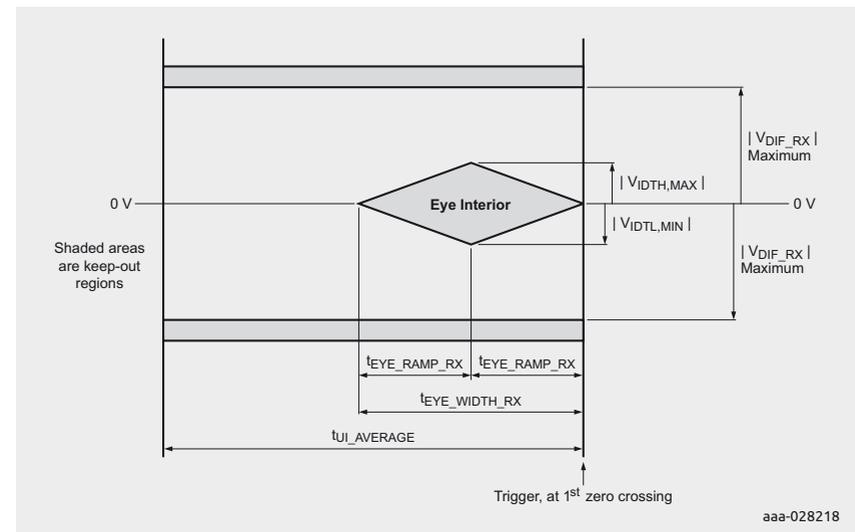

Figure 93 | High speed mode receiver eye diagram for MIPI C-PHY

Figure 94 gives an example of an eye measurement at a C-PHY interface. The signal shows the voltage levels 'Strong 0' and 'Strong 1' as well as 'Weak 0' and 'Weak 1' as to be expected from Table 31. The test scope is triggered at the right side zero crossing behind the open eye.
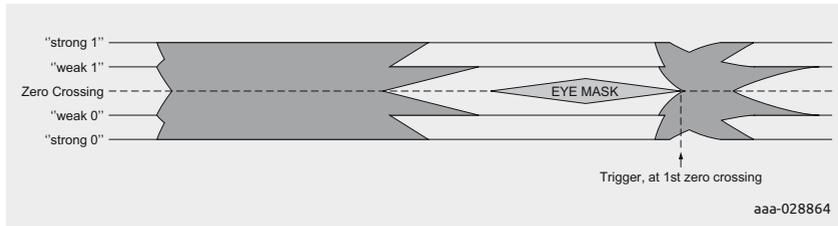

Figure 94 | Eye diagram measurement MIPI C-PHY

8.4 In-vehicle Networking (IVN)

8.4.1 Introduction to In-vehicle Networking

In-vehicle networks consist of multiple microprocessors communicating over different networks. They help manage entertainment and navigation functions or body, motor and safety control as well as lighting and other vehicle systems.

A modern car contains up to 100 ECUs (Electronic Control Units). To exchange all the data between them, several highly reliable IVN protocols (CAN, LIN, FlexRay, Ethernet, etc.) have been designed that can handle the car's physically challenging environment. To ensure safe operation, solutions are required to pass emission and immunity tests, and guarantee signal integrity.

Multimedia bus systems and infotainment networks generally use USB, APIX (Automotive Pixel Link), HDMI or Ethernet, and will adopt USB Type-C.
If two or more microprocessors are communicating, network protocols are necessary that define how data is transmitted. In the next chapters, the most common used networks for automotive vehicles are described, with a focus on the physical layer that defines connectors, cables but also the electrical specification like voltage levels. Only wired networks are considered.

ESD protection diodes for automotive networks must conform with different electrical requirements to those typically found in smartphones or computers. First, ESD diodes need to protect the network and the transceiver pins against ESD strikes. Additionally, the ESD diodes themselves need to be safe against short-to-battery voltages and ensure that communication is not disturbed when the system is tested against EMI. Diode capacitances need a certain matching in differential communication systems and the value of the capacitance needs to be low enough to maintain signal integrity. ESD protection diodes represent a capacitive load on the bus lines, which in differential systems can cause unwanted skew and jitter when not matched properly.

For LIN, CAN or FlexRay networks, typically bi-directional ESD clamping diodes are used. Table 33 gives an overview of the most important interfaces applied in automotive applications.

Table 33: Automotive Interface Overview

Interface	Topology	data rate	specifications/ standards involved	comment
LIN	single wire, power train serves as return path	20 kbit/s	ISO 17987: 2016 [21] SAE J2602 [22]	single master system
CAN (low speed, fault tolerant)	differential two wires, twisted pair; in fault condition single wire	125 kbit/s	ISO 11898, part 3 [23], SAE J2411 [24]	multi master system
CAN (high speed)	differential two wires, twisted pair	1 Mbit/s	ISO 11898, part 2, 5, and 6 [25–27]	multi master system
CAN FD (flexible data rate)	differential two wires, twisted pair	2 and 5 Mbit/s	ISO 11898-1:2015 [28]	multi master system
FlexRay	differential two wires, shielded twisted pair	10 Mbit/s	ISO 17458-4:2013 [29]	multi master system
BroadR-Reach, 100BASE-T1 (Ethernet)	two wires, unshielded twisted pair cable	100 Mbit/s	Open Alliance [30] IEEE STD 802.3 [31]	multi master system

8.4.2 LIN Interface

The first Local Interconnect Network (LIN) specification was published in 2003 by the LIN consortium, which concluded its work with the finalization of the LIN Specification 2.2.A in 2010. Conformance test specifications are now part of the ISO 17987:2016 [21] and the latest revision of SAE J2602 [22]. This is a subset of specifications taken from the LIN Specification 2.0.

LIN is a concept for low cost automotive networks. It is typically used where the higher data rates and versatility of the CAN network is not required. It connects modules into a sub-bus that is connected to the existing CAN network. Typical modules where LIN is used are seats, locks, mirrors, or as interface to sensors, for instance rain detectors. It uses a single wire, serial communication protocol and operates at low speed, with a maximum data speed of 20 kbit/s. The bus voltage level is approximately the supply voltage, in 12 V board net typically 12 V.

External ESD protection on the LIN bus connection is recommended by LIN transceiver suppliers for extending the ESD voltage level the module can withstand. Relevant electrical parameters for selecting external ESD protection diodes include the diode's breakdown and working voltages, V_{BR}, V_{RWM}, and capacitance C_d.

In addition, ESD protection diodes should be chosen to withstand the maximum battery voltage without being damaged, in case the LIN bus line is shorted to the battery line. For a 12 V board net the maximum battery voltage is 16 V. The operating voltage range for an ECU is defined between 8 V and 18 V, referenced to the local ECU ground. From this range definition, V_{RWM} should be bigger than 18 V. Typically, bi-directional ESD diodes are used for LIN bus application with a breakdown voltage bigger than +/– 27V because of the following aspects.

Diode capacitance C_d has to be smaller than 100 pF to maintain signal integrity at the maximum data rate of 20 kbit/s. To minimize the total impact of the diode on the system C_d should be smaller than 30 pF.

LIN bus uses single-ended transmission and during EMC tests the voltage levels of, e.g. capacitively coupled RF signals, can exceed the diode's breakdown voltage. With voltage exceeding the breakdown voltage of the ESD protection diode, the communication signal is clamped to the diode's clamping voltage V_{CL}. The higher the breakdown voltage, the later the EMC test levels will start to have an influence, i.e. disturbing the dominant and recessive voltage levels. The total system is more robust against inducted noise and EMI. With diodes having a $V_{BR} \geq 27$ V, modern transceiver modules pass typical EMC tests as required by the automotive industry.

To avoid impacting the module's EMC performance, it can be stated that the higher the breakdown voltage the better. On the other hand, sufficient clamping performance for ESD events has to be achieved.

Figure 95 depicts a LIN bus with a single bidirectional ESD diode to protect the single LIN data signal.
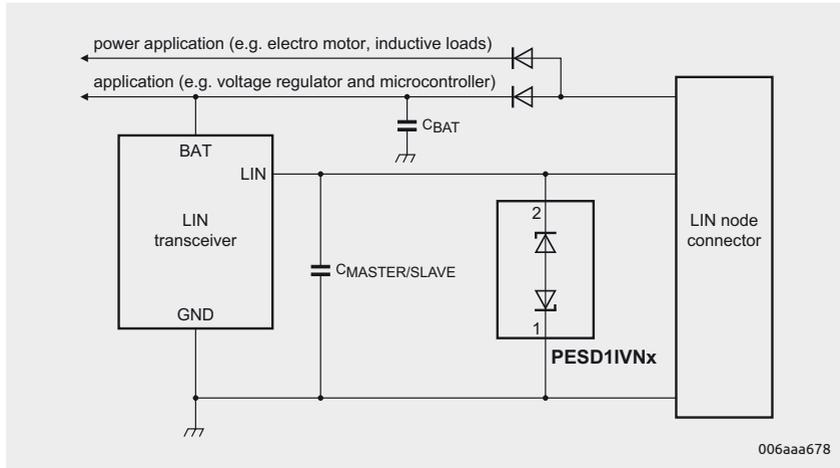
Figure 95 | LIN system architecture with a single ESD protection device to protect the LIN node

8.4.3 CAN Interface

Developed in the 1980s by Robert Bosch GmbH, the Controller Area Network (CAN) specification became an ISO standard [23–27] in the early 1990s.

CAN is a very well-established network for automotive and is considered more flexible, but more expensive, than LIN. A CAN network typically uses a two wire, twisted pair cable to transmit and receive serial data. High-speed CAN (parts 2, 5, and 6 of the ISO 11898), specifies transmission rates up to 1 Mbit/s. Low-speed, fault-tolerant CAN (part 3 of the ISO 11898), specifies up to 125 kilobits per second. Fault tolerant often means that the transceiver can switch from a differential receive and transmit capability to a single-wire transmitter and/or receiver in error conditions. This means single ended (fault tolerant) +12 V bus voltage max, and differential −12 V bus voltage maximum.

A CAN transceiver provides the physical link between the protocol controller and the physical bus wires in a network. CANL is the LOW-level CAN bus line. In normal operating mode, the value of dominant state is about 1.4 V and the value of recessive state is 5 V. In low-power modes, the voltage of CANL is equal to the battery voltage. CANH is the HIGH-level CAN bus line. In a typical operating mode, the value of dominant state is about 3.6 V and the value of recessive state as well as in low-power modes is 0 V.

External clamping circuits can be applied to the CANH and CANL line to extend the ESD robustness of the network, protect the CAN transceivers and ensure communication. The industry offers devices specifically designed to protect two CAN bus lines from damage caused by ESD and other transients.

As CAN networks may be shorted to voltage sources, e.g. the car battery, ESD protection devices at the CANL and CANH lines must be able to withstand the higher voltage levels. In jump-start conditions, or two 12 V batteries in series, this means that a minimum of 2 × 12 V is required as stand-off voltage VRWM. Maximum data rate for CAN is 1 Mbit/s.

8.4.4 CAN FD Interface

Because more and more ECUs are used in an automotive network with the requirement to transmit and receive more data, the classical CAN network with its limitation to 1 Mbit/s is considered insufficient for future needs. CAN FD is an update of the physical layer of CAN [28].

A major difference is a flexible data rate, that is defined up to 5 Mbit/s. 2 Mbit/s is the typical implementation limit suitable for many applications that do not require higher data rates.

Figure 96 shows a CAN bus example with different node options. Node 1 shows a subsystem with microcontroller connected via a CAN controller and a CAN transceiver to the bus. For Node 2 a microcontroller with built-in CAN controller is used, whereas for Node N a CAN I/O Expander is attached to the bus providing extra I/Os, pulse width modulated outputs or ADC inputs for general usage.
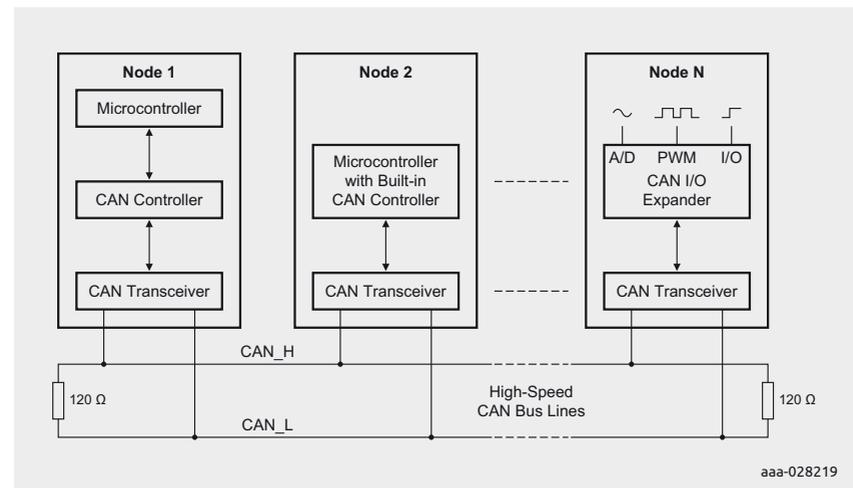

Figure 96 | CAN Node configuration options

Figure 97 explains the CAN bus logical states Dominant and Recessive in low-speed mode. A Dominant state can overwrite a Recessive state. The Recessive state is the idle state of the interface and represents logical 1. In Recessive state, CAN_H has a nominal voltage of 0 V and CAN_L has a voltage of 5 V.

The signal line CAN_H toggles between the single-ended low state voltage of 0 V and a high state voltage of 3.6 V. The CAN_L signal has a low level of 1.4 V and a high level of 5 V. So both lines have a nominal swing of 3.6 V. For the logic state, Dominant CAN_H is bigger than CAN_L for a differential receiver whereas in Recessive state CAN_H is lower than CAN_L.

In Figure 98 the Highspeed CAN bus voltages are depicted. In idle state or Recessive state both signal lines have a voltage level of about 2.5 V. In Dominant state CAN_H jumps up to 3.5 V and CAN_L goes down to 1.5 V, creating a differential voltage of 2 V.

Normally the CAN bus receivers exploit the differential voltage on the CAN lane. For low-speed the receivers can switch to a mode where data reception is based on a single line only. This is a fallback mode if one of the signal lines is broken. The single line mode is called Limp-Home-Mode.
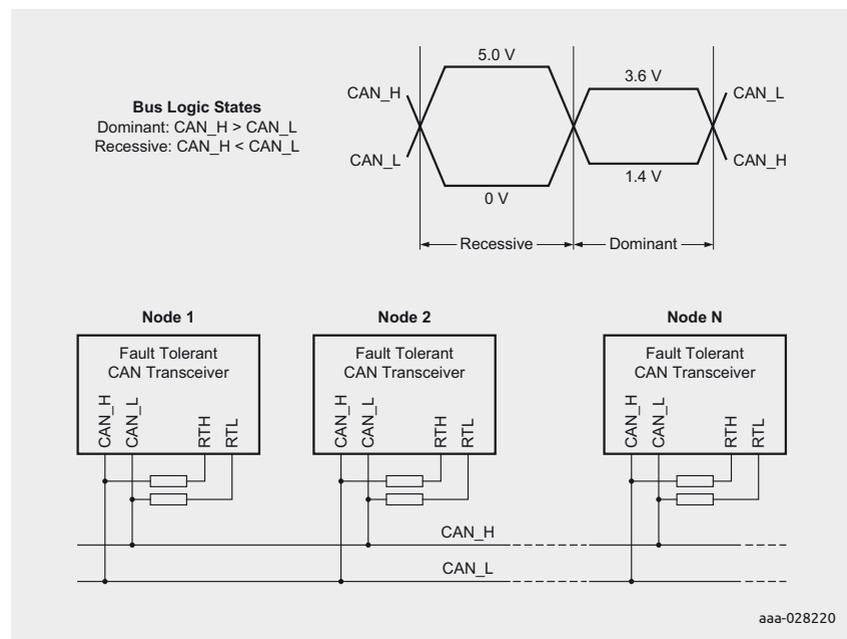

**Figure 97** | Low speed CAN Bus logical states
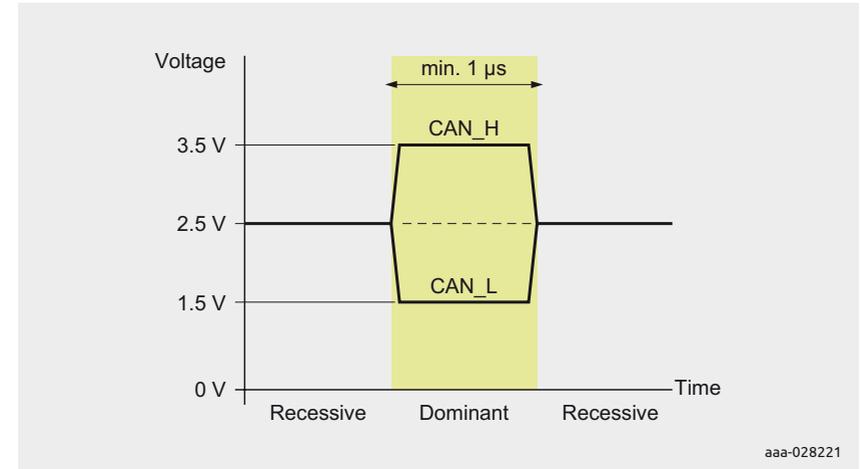
Figure 98 | High speed CAN Bus logical states

8.4.5 FlexRay Interface

Developed since 1999 by the FlexRay Consortium [29], the first FlexRay systems were introduced in 2006. It is a fault-tolerant and high-speed bus system, targeted at the growing networking demands in Automotive, and suited for applications like X-by-Wire.

FlexRay can operate up to 10 Mbit/s per channel, using the differential signals BP and BM. In addition to single-channel operation (like LIN and CAN), it can be operated as a dual-channel system, making data available in a redundant network. The higher fault tolerance and higher transmission rates of FlexRay systems lead to higher system costs compared to CAN and LIN protocol-based networks.

For ESD protection diodes, typically low diode capacitance of < 20 pF is required, with a matching of about 2%.

Figure 99 shows a FlexRay transceiver that is coupled via a common mode choke, a differential termination with twice RT/2 and a bidirectional ESD protection to the bus.
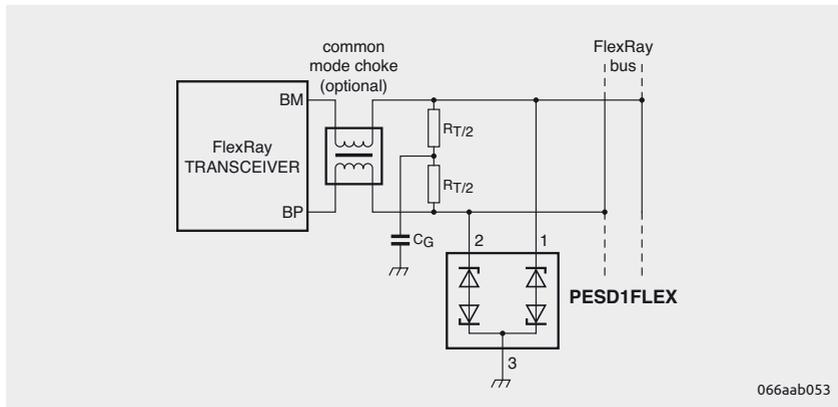
Figure 99 | FlexRay transceiver coupled to the FlexRay bus

8.4.6 BroadR-Reach and 100BASE-T1 Interface

Automotive Ethernet 100BASE-T1 and BroadR-Reach provide 100 Mbit/s transmit and receive capability over a single unshielded twisted pair cable. The standard BroadR-Reach has been defined by Broadcom and has been transferred into the OPEN Alliance Special Interest Group [30]. Ethernet is seen as a universal and flexible alternative to CAN or FlexRay networks. It is used for modules that need to process more data, and need higher data rates, like camera, driver assistance and back-bone networks. For next car generations, automotive-suitable gigabit Ethernet is being investigated.

Today's automotive Ethernet is AC-coupled, mainly like depicted in Figure 100. This allows to use protection devices with low VBR, suitable to the PHY. The internal ESD protection of modern 100BASE-T1 PHYs triggers at 10-14V. Hence, a protection device with lower trigger voltage should be chosen.
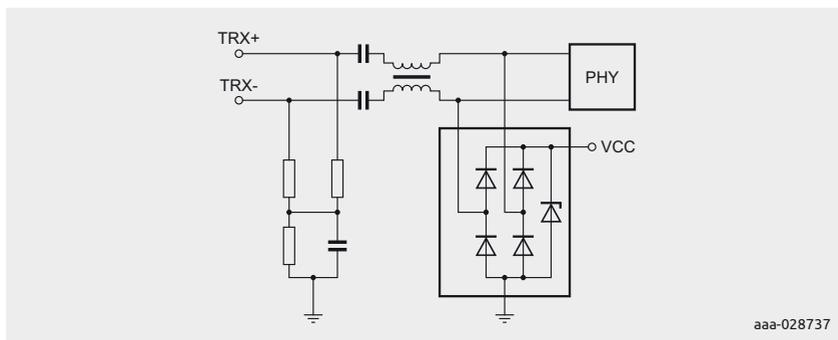

Figure 100 | Ethernet Link

8.4.7 Automotive Multimedia Interfaces

Despite dedicated IVN technologies designed for the reliable connection of electromechanical devices and modules in the car, many buses are also used in the multimedia systems of modern cars. Besides technologies that are also used in the communication segment, like USB and HDMI, there are dedicated automotive multimedia buses like APIX. When using high-speed buses known from communication and computing in the automotive environment, individual components need to meet higher quality standards. Furthermore, functional requirements occasionally change, like short-to-battery scenarios.

Automotive multimedia interfaces from computing

Usually buses that are known from computing are used in automotive applications within the multimedia environment. As this is a non-safety related application, sometimes the same protection strategies and devices can be used. Sometimes, the high quality standards which are common in automotive also apply to the entertainment system. In this case, all involved semiconductor devices including the protection devices must fulfill AEC-Q100/101. The qualification implies high quality and reliability of the devices and does not change the topology.

Dedicated automotive multimedia interface APIX

APIX stands for Automotive Pixel Link. The interface was designed by Inova Semiconductors and licensed in 2008 by Fujitsu. It can be used to transmit digital video signals over a distance up to 15 m. By design, it is a point-to-point topology. Third generation APIX3 has been available since 2016. Since APIX2 it supports bi-directional protocols in addition to one-direction video transmission. APIX2 support a 720p video signal and additional communication over SPI, I2C, or Ethernet over the same interface. APIX3 supports data rates up to 6 Gbit/s. Depending on the operation mode, one or two shielded two-wire twisted-pair (STP) or shielded quad-wire twisted pair are required. Furthermore, it allows data lines to be used as power supply for the modules.

To protect an APIX data line against ESD, state-of-the art protection technology is required. Protection devices used in the computing segment to protect high-speed data lines with extremely low capacitance are suitable for this task. In the case of power over cable, protection devices from computing are not suitable, as the breakdown and snap-back voltages are often too low. A dedicated solution is needed, like the PESD18VF1BL, which have a high breakdown voltage while the capacitance is extremely low.

8.5 Antenna interfaces

8.5.1 Properties of antenna interfaces

RF antennas are the interface between electromagnetic waves and electrical current. Independent of whether the antenna is receiving or transmitting, any component that is added to the antenna system should not interfere with the signal, to maintain the optimum transmission or reception performance.

If an antenna is removable or if there is a need for factory programming and tuning, antenna connectors are used. These connectors give ESD discharges an entry point into the system. Even though antennas may sometimes seem completely hidden inside a device's case, there are still numerous instances where internal antenna connectors are used. Such internal antenna connectors may be subject to ESD discharges during device assembly.

Figure 101 | Removable Antenna

If an ESD event occurs at an antenna terminal, it can cause severe damage to the sensitive circuitry. Thus, external ESD protection is strongly recommended to achieve good ESD robustness.

Figure 101 shows an F-Connector interface for a removable antenna. Figure 102 gives an example of internal antenna contacts as an interconnect to another board that can be seen in many smartphone applications. An internal antenna terminal is illustrated in Figure 103.
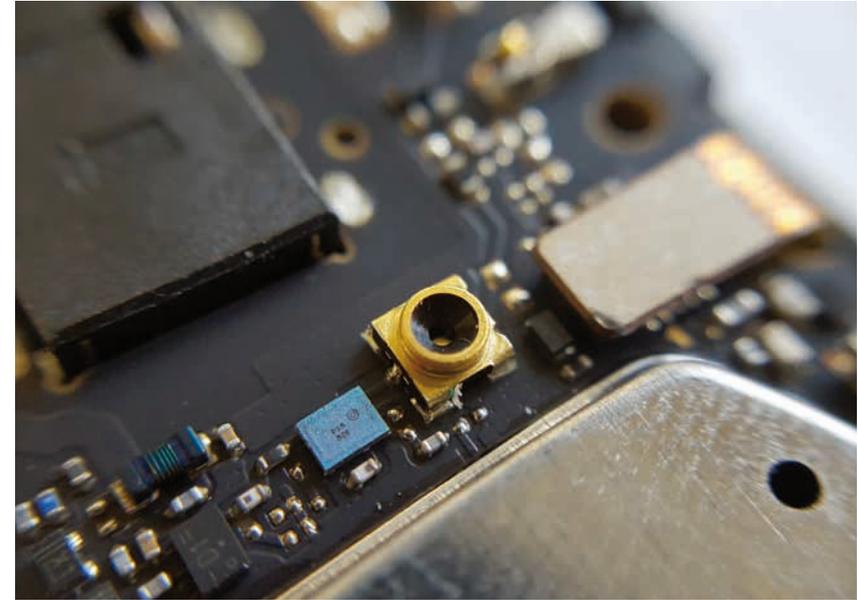

Figure 102 | Internal antenna contacts
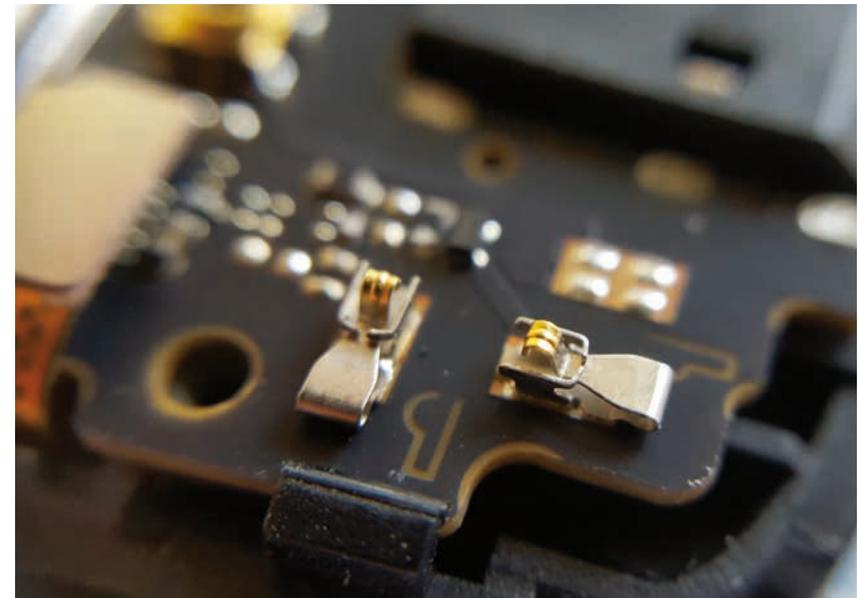
Figure 103 | Internal antenna terminal

8.5.2 ESD protection for antenna interfaces

What properties are required for a protection device applied at an antenna terminal?

Firstly, a protection device should not limit the signal amplitude with its clamping characteristics. Thus, the breakdown voltage and subsequently the maximum reverse working voltage V_{RWM} should be larger than the maximum signal amplitude at the antenna terminal.

It is inevitable that a protection device has a capacitance. To minimize the impact of the ESD protection capacitance it should not limit the RF signal's high frequencies, therefore the capacitance should be as small as possible. The C_d over voltage curve should be as flat as possible in the target frequency band of the application. Besides low capacitance it should also have a high linearity to avoid distortion.

8.6 Supply line protection with TVS diodes

8.6.1 Introduction to supply line protection

Transient voltage suppressors (TVS) protect other than data lines against overvoltages. When placed on a signal or supply line connected to a sensitive component (e.g. a highly integrated SoC), harmful overvoltages can be discharged through the protection device.

Sources of high current surge pulses can be of external or internal. External surge events can originate from, for example, an external power supply or a discharge event from a charged cable. Internal surge events can originate from sources such as switching events or load changes.

The Nexperia terminology denotes the difference between ESD protection products and TVS products. Namely, TVS protection devices (or PTVS) can withstand significantly higher energy originating from high current surge pulses and are meant to be placed on supply lines. In literature, and by some protection device suppliers, both protection devices can be classified as TVS.

8.6.2 Pulse standards

Depending on the source of the pulse it may have different pulse shapes (i.e. pulse length and rise/fall times) and energy. Common surge pulse standards are described in Chapter 7. It is worth noting that although standards like IEC 61000-4-5 are intended to describe the direct or indirect effect of lightning strikes to power lines, devices that are tested to this standard are not subject to these events. The test methods are used to characterize device robustness against other events that contain a similar amount of energy and have similar pulse shape.

8.6.3 TVS operation

As long as the voltage on the protected line stays below the breakdown voltage of the TVS diode, it does not react. Once the voltage on the line reaches the protection device's breakdown voltage, it will start conducting current to ground resulting in the voltage to be clamped to V_{CL}.
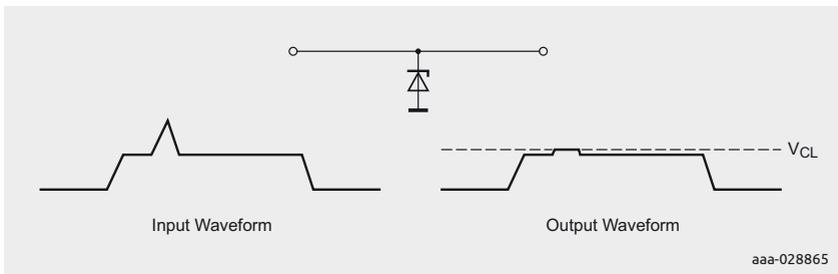

Figure 104 | Operation of a TVS diode on signal line

Based on fundamental parameters of a TVS protection device (mainly breakdown voltage Vbr and dynamic resistance R_{dyn}—see Chapter 2 for details), the clamping voltage for the peak current of a pulse can be calculated by

$$V_{CL} = I_{PP} \cdot R_{dyn}$$

8.6.4 Typical applications in a portable device

As surge events are commonly expected to enter a portable device using the power (charger) input, this is the most prominent place where TVS protection is applied. Figure 105 illustrates this. Optionally there may be a need to add a secondary protection behind the charger switch or overvoltage protection (OVP) to protect the adjacent charger or power management components.

Due to increasing sensitivity of internal system blocks in a battery-operated device, it additional TVS protection components may be required at the point of load. This helps to protect sensitive system blocks against harmful surge events that may occur on internal supply lines.
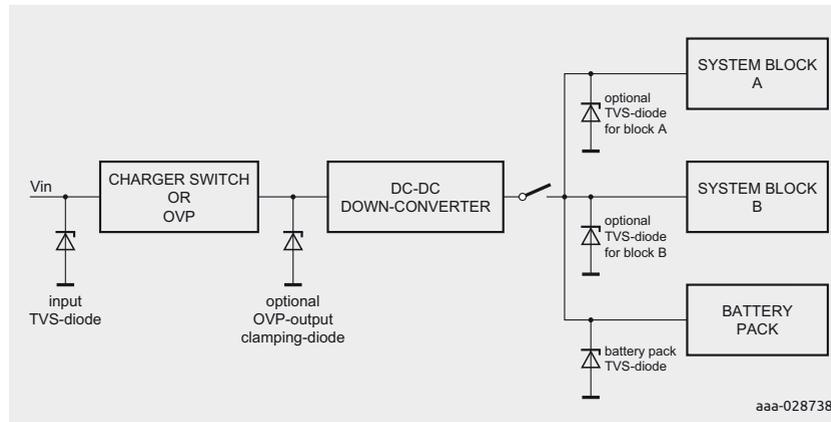

Figure 105 | Example of a charger path with protection diodes at typical locations

Chapter 9
Summary

Due to IC miniaturization, the high-speed interfaces commonly used in mobile communication and computing equipment are more sensitive to ESD strikes and surge events. The high data rates that need to be processed demand a larger passband of the IC input structures. This makes the design of robust I/O structures more sophisticated, and advanced external ESD protection a requirement.

The new sensitivity needs to be well managed by the ESD protection devices. This is achieved by low clamping voltages, low dynamic resistance and low parasitic impedances inside the package technology. Snap-back technology allows very low clamping voltages. High switching speed is another important requirement for devices using this topology, helping avoid interface damage caused by surge events.

In today's automotive applications, modern communications and multimedia devices require high speed data as well. The overall trend for more driver assistance systems, advanced safety systems, enhanced connectivity and in-vehicle networks asks for better surge, EMI and ESD protection.

The introduction of new power delivery concepts like USB PD, and new connectors like USB-Type-C, demand new solutions in protecting the power path itself or to safeguard against short circuits.

The selection of suitable external protection devices and a proper system design has become more important for all electronic designs. Proper placement of ESD protection and the SoC help to dissipate surge energy in the protection device. The use of common mode filters in combination with modern ESD protection technology improves system level robustness even further. Nexperia provides a full portfolio of protection products to ensure robust and safe devices, and help eliminate field returns in all application areas.

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Abbreviations

Abbreviations

AC	Alternating Current
APIX	Automotive Pixel Link
CAN	Controller Area Network
C_d	Diode Capacitance
CEC	Consumer Electronics Control
CMC	Common Mode Choke
CMF	Common Mode Filter
C_t	Tip Capacitance
DC	Direct Current
DP	Display Port
DUT	Device Under test
ECU	Electric Control Unit
EMI	Electromagnetic Interference
EOP	End Of Packet
ESD	Electrostatic Discharge
f_{-3dB}	Frequency with -3dB attenuation/loss
FET	Field-effect Transistor
GND	Ground (rail)
GPS	Global Positioning System
GSM	Global System for Mobile Communication
HBM	Human Body Model
HDCP	High-bandwidth Digital Content Protection
HDMI	High Defintion Multimedia Interface
HMM	Human Metal Model
IC	Integrated Circuit
I_{hold}	Hold Current
I_{PPM}	Peak Pulse Current, single pulse
I_{RM}	Leakage current at VRWM
LIN	Local Interconnect Network
MIPI	Mobile Industry Processor Interface
MOSFET	Metal oxide semiconductor field-effect transistor
NRZ	Non Return to Zero (Code)

NRZI	Non Return to Zero Inverted (Code)
OVP	Over Voltage Protection
PCB	Printed Circuit Board
RD	Running Disparity
R_{dyn}	Dynamic Resistance
RF	Radio Frequency
RX	Receiver Input
S_{21}	Insertion loss (scattering parameter)
SCR	Silicon Controlled Rectifier
SE0	Single Ended Zero
SEED	System Efficient ESD Design
SoC	System on Chip
STP	Shielded Two-wire Twisted-pair
TDR	Time Domain Reflection
T_j	Junction Temperature
TLP	Transmission-Line Pulse
TMDS	Transition Minimized Differential Signal
TX	Transmitter Output
USB	Universal Serial Bus
V_{BR}	Breakdown Voltage
V_{CL}	Clamping Voltage
V_{conn}	5 V voltage on connection channel Type-C
V_{ESD}	Maximum ESD Voltage
V_F	Forward Voltage
V_{hold}	Hold Voltage
VF-TLP	Very Fast Transmission Line Pulse
V_{RWM}	Stand-off Voltage, max. operation voltage
WiFi	Wireless local area network (Artificial abbreviation)
WL-CSP	Wafer-level Chip Scale Package
XOR	Ex-Or, logical function

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Design Engineer's Guide

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September 2018

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ISBN: 978-0-9934854-3-5